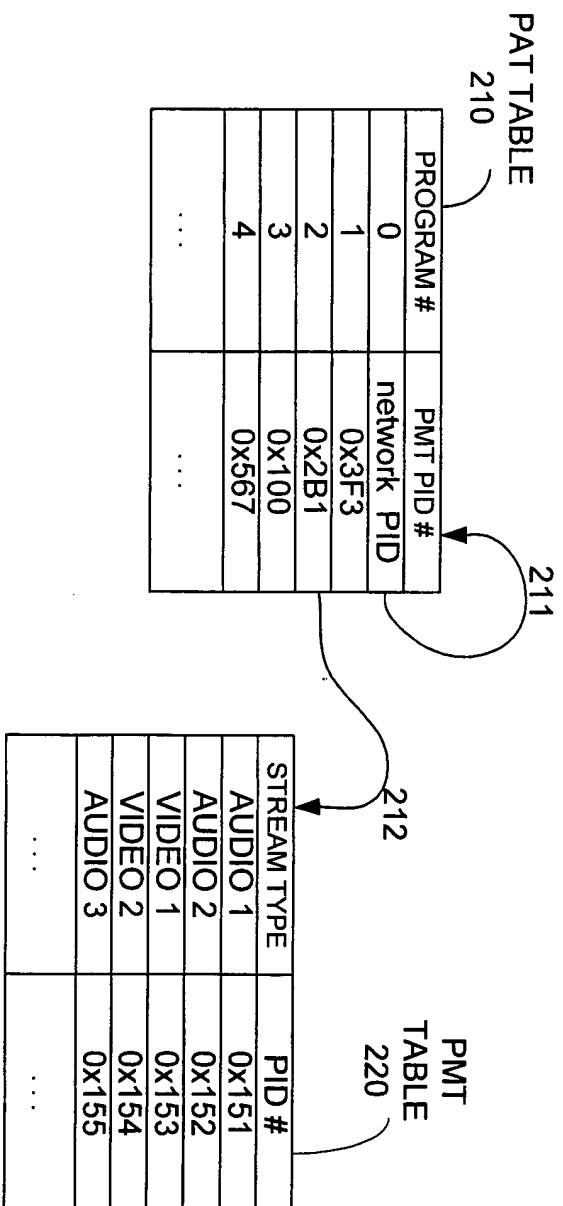


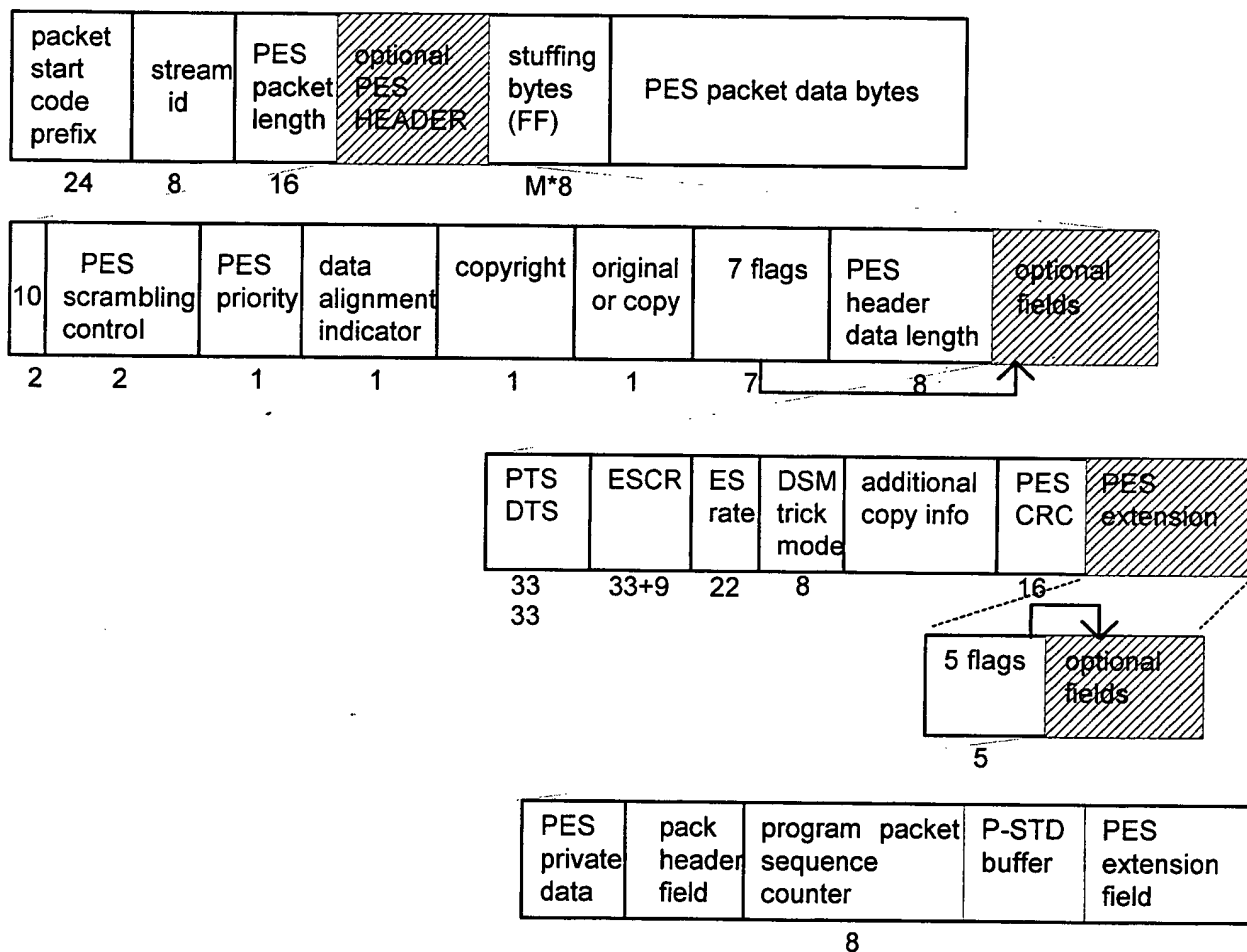
--PRIOR ART--

FIGURE 1



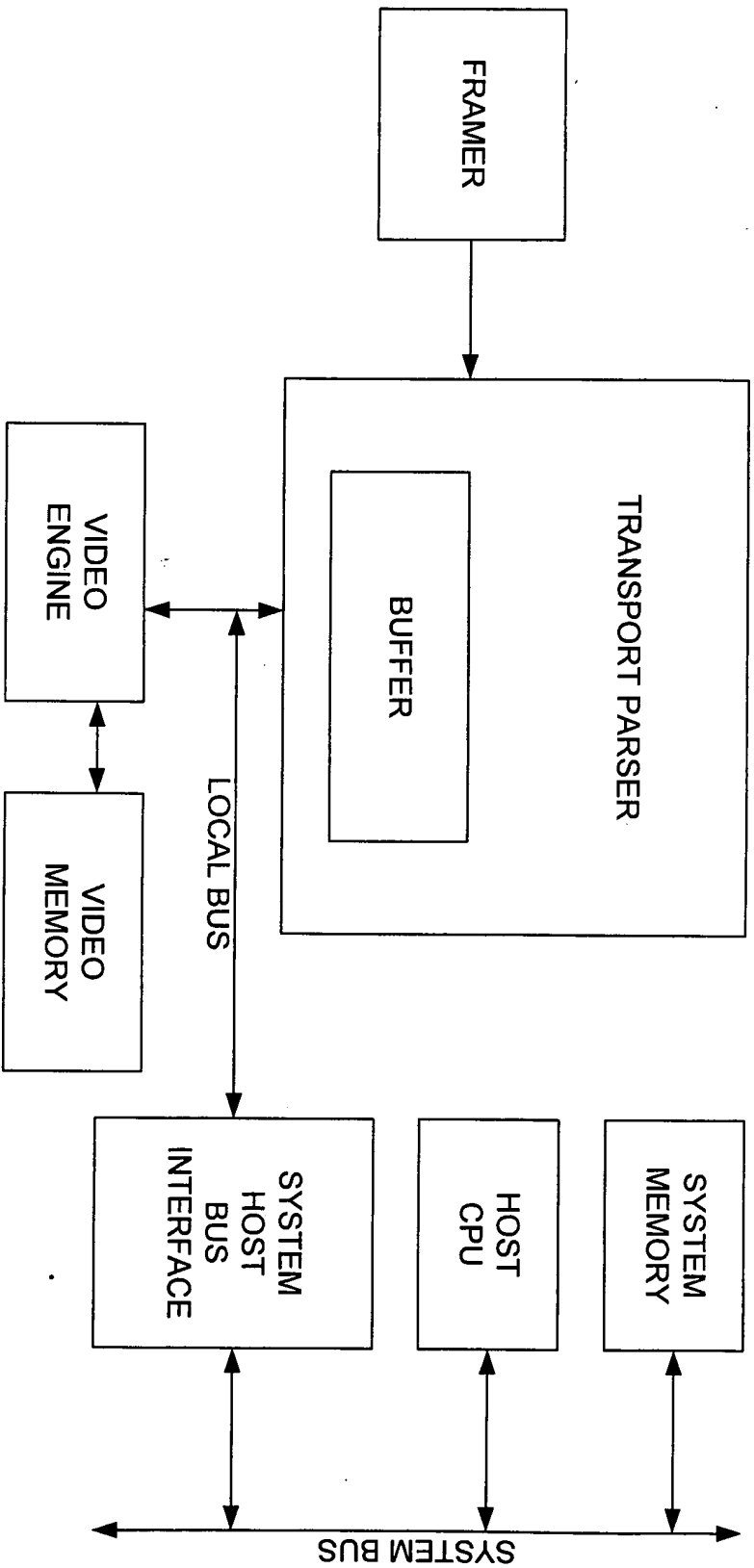
--PRIOR ART--

FIGURE 2



--PRIOR ART--

FIGURE 3



-- PRIOR ART --
FIGURE 4

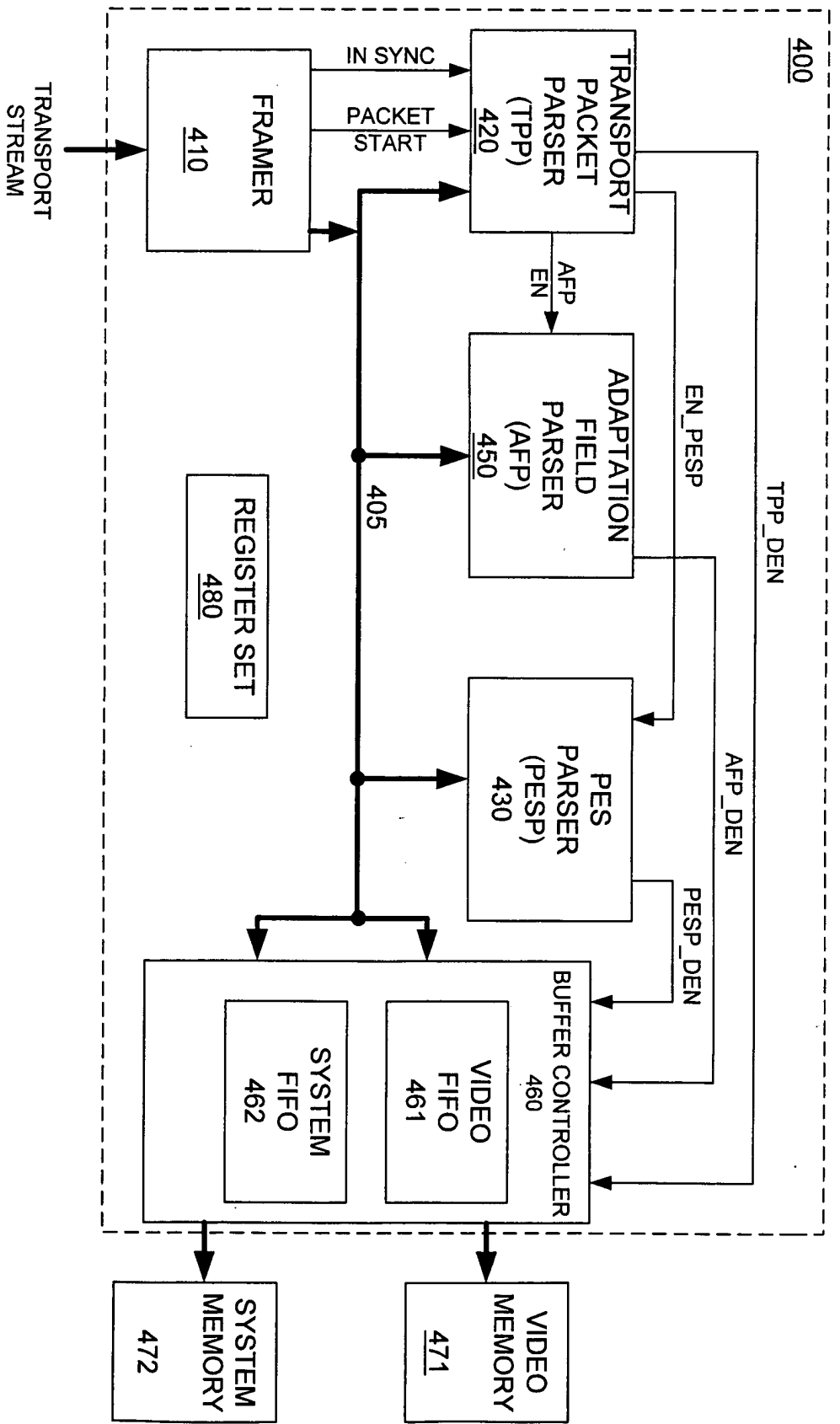


FIGURE 5

FIGURE 5 is a block diagram of a video processing system 400. A TRANSPORT STREAM enters a FRAMER 410. The FRAMER outputs IN SYNC and PACKET START signals to a TRANSPORT PACKET PARSER (TPP) 420. The TPP outputs an AFP_EN signal to an ADAPTATION FIELD PARSER (AFP) 450. Both the TPP and AFP output to a common bus 405. The bus 405 also receives signals from a REGISTER SET 480 and outputs to a BUFFER CONTROLLER 460. The BUFFER CONTROLLER contains a VIDEO FIFO 461 and a SYSTEM FIFO 462. The TPP also outputs EN_PESP and AFP_DEN signals to the BUFFER CONTROLLER. The BUFFER CONTROLLER outputs to VIDEO MEMORY 471 and SYSTEM MEMORY 472.

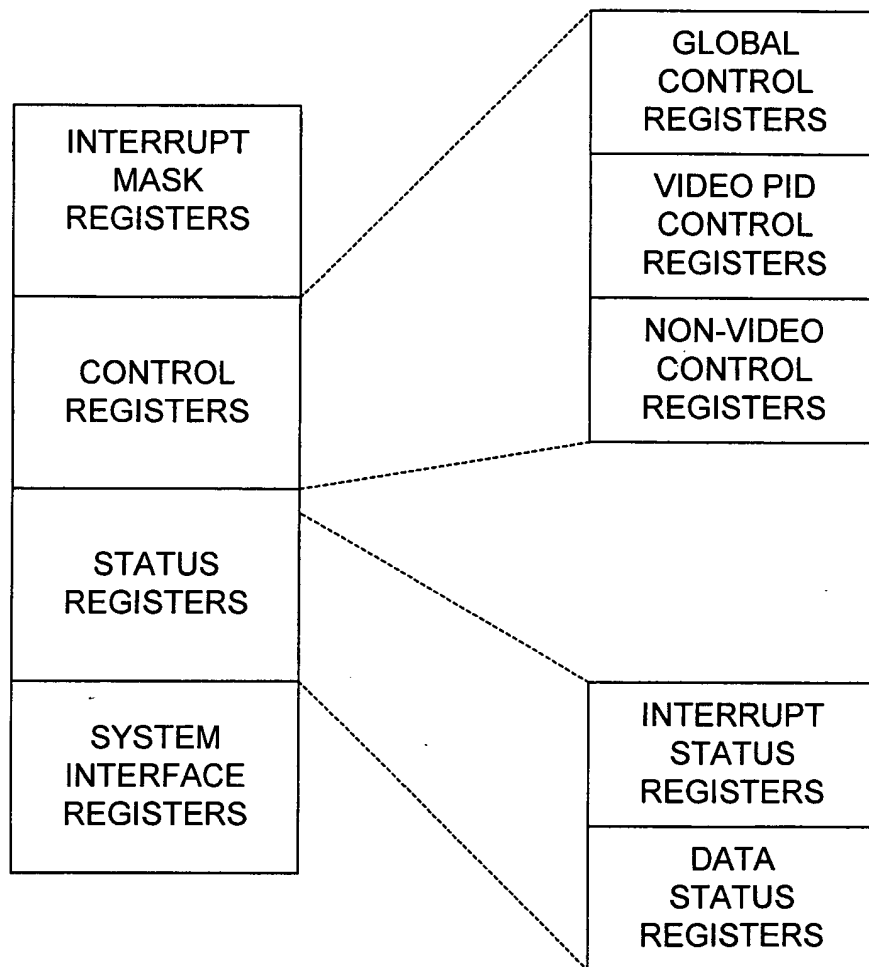


FIGURE 6

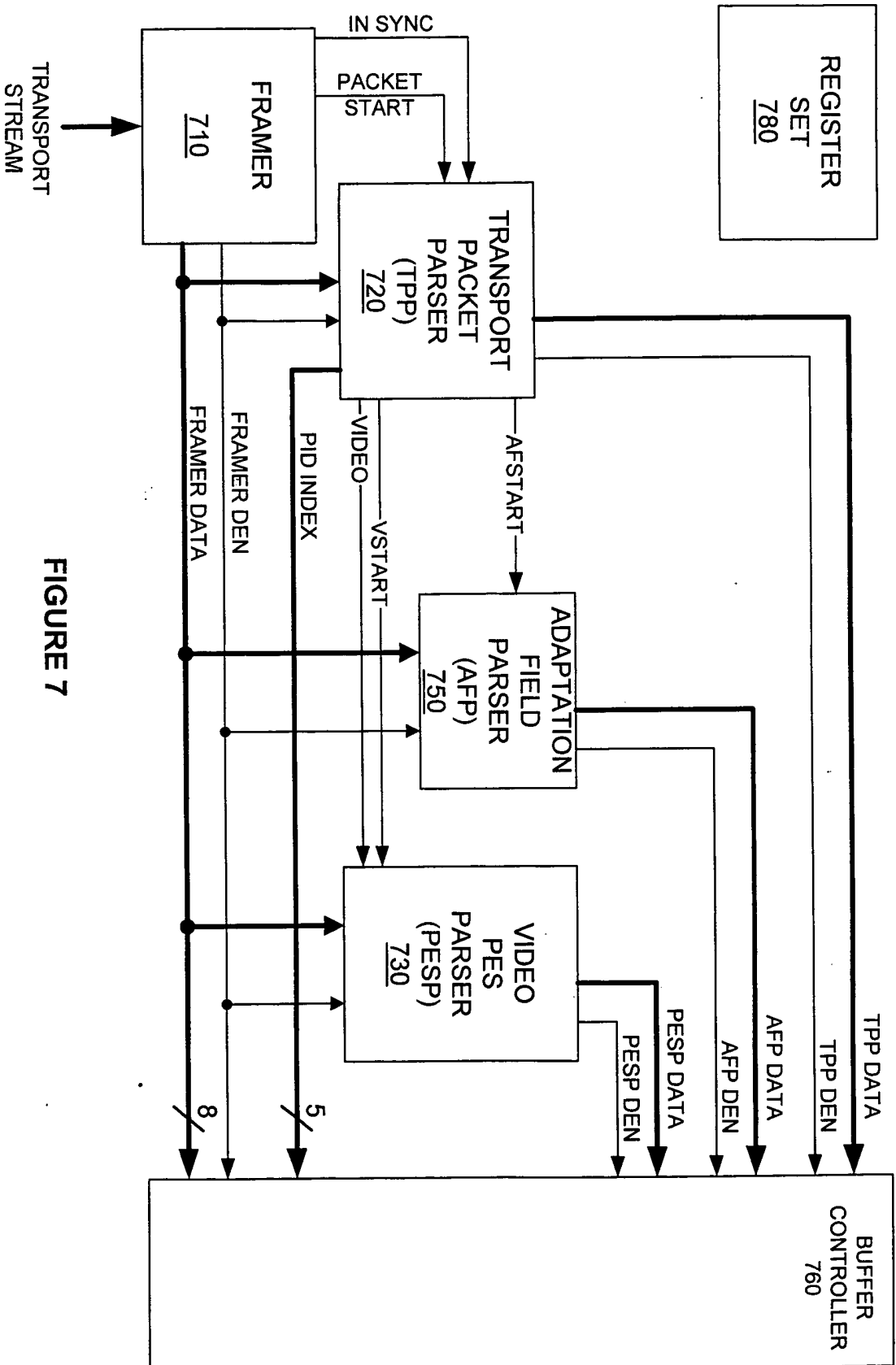


FIGURE 7

FIGURE 7 is a block diagram of a video processing system. The system includes a REGISTER SET 780, a TRANSPORT PACKET PARSER (TPP) 720, a FRAMER 710, an ADAPTATION FIELD PARSER (AFP) 750, a VIDEO PES PARSER (PESP) 730, and a BUFFER CONTROLLER 760. The REGISTER SET 780 provides a PACKET START signal to the TPP 720 and an IN SYNC signal to the FRAMER 710. The FRAMER 710 receives a TRANSPORT STREAM and outputs data to the TPP 720. The TPP 720 outputs AFSTART to the AFP 750 and VIDEO and PID INDEX signals to the PESP 730. The AFP 750 outputs AFP DATA and AFP DEN signals to the BUFFER CONTROLLER 760. The PESP 730 outputs PESP DATA and PESP DEN signals to the BUFFER CONTROLLER 760. The BUFFER CONTROLLER 760 receives TPP DATA, TPP DEN, AFP DATA, AFP DEN, PESP DATA, and PESP DEN signals. The FRAMER 710 also outputs FRAMER DEN and FRAMER DATA signals to the TPP 720. The FRAMER DATA signal is divided into three paths: a 5/ path to the TPP 720, a 5/ path to the AFP 750, and an 8/ path to the TPP 720.

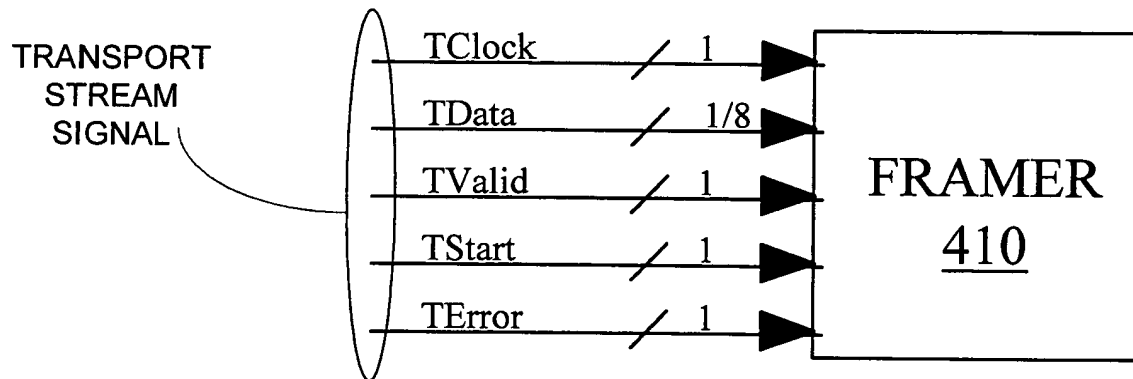


FIGURE 8

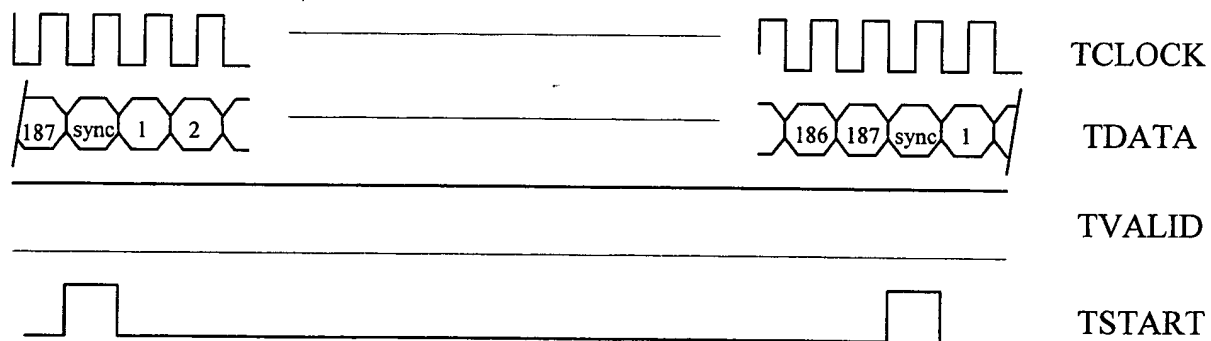
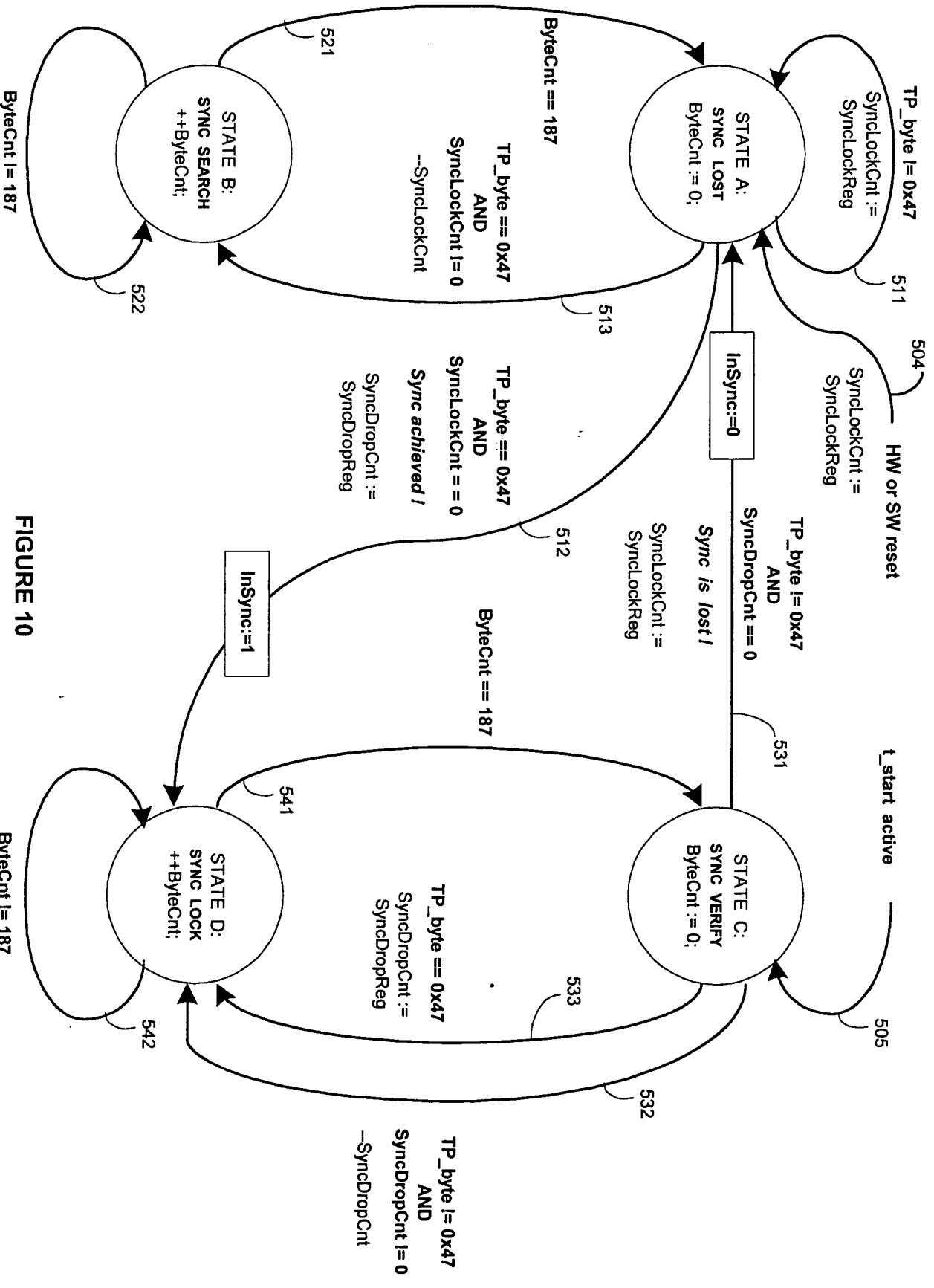


FIGURE 9



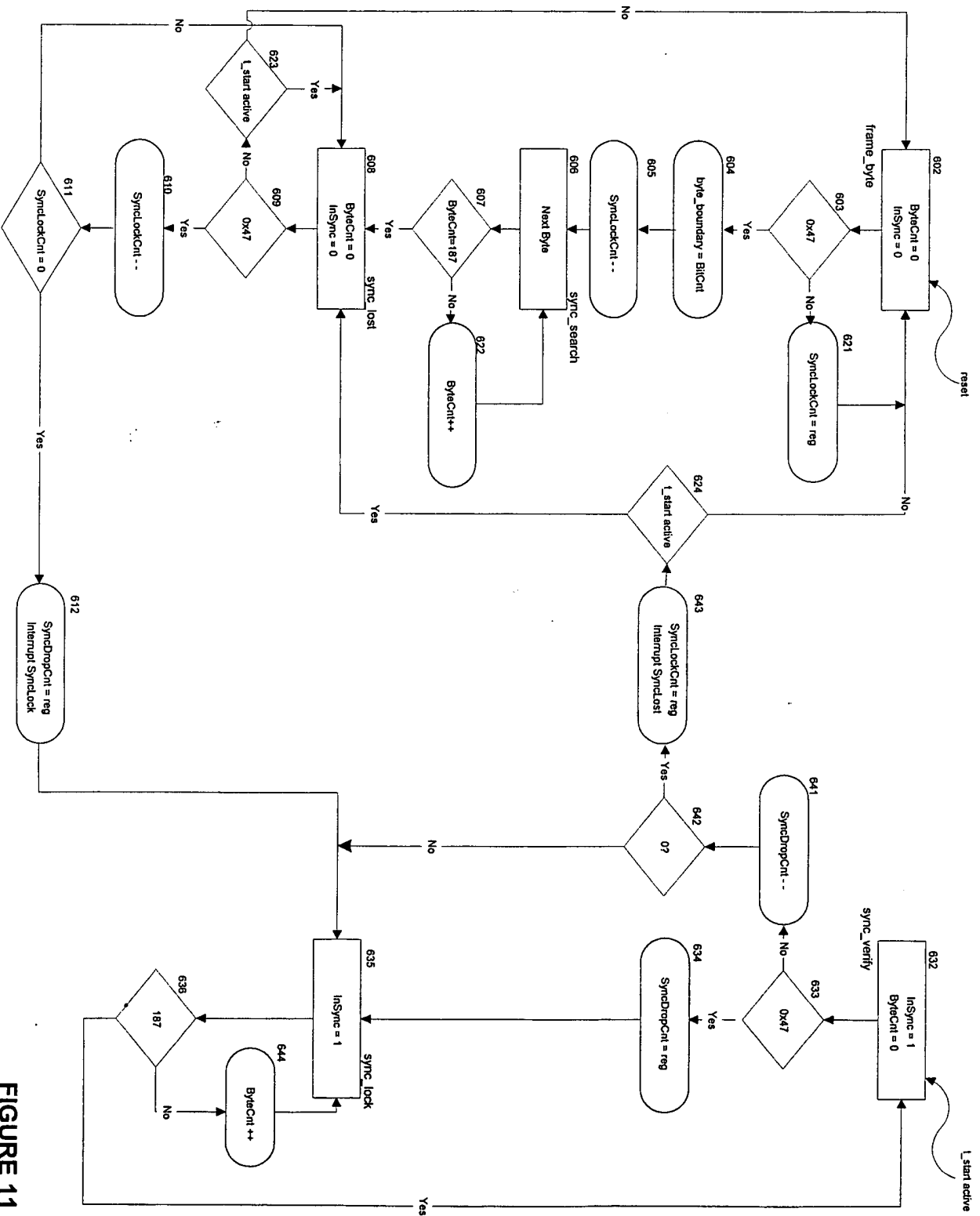


FIGURE 11

Transport Demultiplexer Global Status Register					
Field Name	Bits	Len	Default	Type	Description
FramerSyncLock	0	[1]	0	R/W	This bit is set to '1' after the frame synchronization has been acquired. WR_ACC_CLEAR.
FramerSyncDrop	1	[1]	0	R/W	This bit is set to '1' after the frame synchronization has been lost. WR_ACC_CLEAR.
CurrentFramerState	20-22	[3]	'000'	R	<p>This 3 bit field codes the current state of the framer:</p> <p>'000' – Capturing a byte '001' – Out of TP frame synchronization '010' – Searching for synchronization '011' – Checking for synchronization '100' – In the TP frame synchronization</p> <p>NOTE: Only a framer state machine updates this field. Write access does not modify it.</p>
UnusedField	29-31	[3]	'000'	R/W	Unused and reserved field.

FIGURE 12

Transport Demultiplexer Interrupt Mask Register					
Field Name	Bits	Len	Default	Type	Description
EventInterruptMask	0-18	[19]	0	R/W	If set to '1' enables local sources of interrupts. Bit 0 – FramerSyncLock Bit 1 – FramerSyncDrop Bits 2 – 19 Other Functionality
EnableGlobalDemuxInterrupt	20	[1]	0	R/W	If set to '1' enables globally TD core interrupts.
UnusedField	21-31	[11]	0	R/W	Unused and reserved field. Always set to 0.

FIGURE 13

Transport Demultiplexer Global Control Register					
Field Name	Bits	Len	Default	Type	Description
FramerSyncLockLength	0-4	[5]	00101	R/W	Five bits field to select a number of consecutive transport packets after MPEG-2 frame (bit-stream) synchronization is declared.
FramerSyncDropLength	5-7	[3]	011	R/W	Three bits field to select a number of consecutive transport packets after a loss of MPEG-2 frame synchronization is declared.
FramerBitPolarity	8	[1]	0	R/W	'0' selects msb first (default mode), '1' select lsb first
FramerClockPolarity	9	[1]	0	R/W	If set to '0' framer will latch on falling edge (default) If set to '1' framer will latch on rising edge.
FramerMode:	10-11	[2]	'00'	R/W	Defines a combination of external control signals: '00' – Framer uses T_start only. '01' – Framer uses T_valid only. '10' – Framer uses T_start and T_valid. '11' – Framer uses T_clock and T_data only.
Other Functionality Bits	12-15	[4]			Other functionality (not relevant to Framer)
T_ValidPolarity	16	[1]	1	R/W	'1' selects active high [5V] for t_valid external signal
T_StartPolarity	17	[1]	1	R/W	'1' selects active high [5V] for t_start external signal
T_ErrorPolarity	18	[1]	1	R/W	'1' selects active high [5V] for t_error external signal
Other Functionality Bits	19-28	[10]			Other functionality (not relevant to Framer)
UnusedField	29 -31	[3]	0	R/W	Unused and reserved field. Always set to 0.

FIGURE 14

720

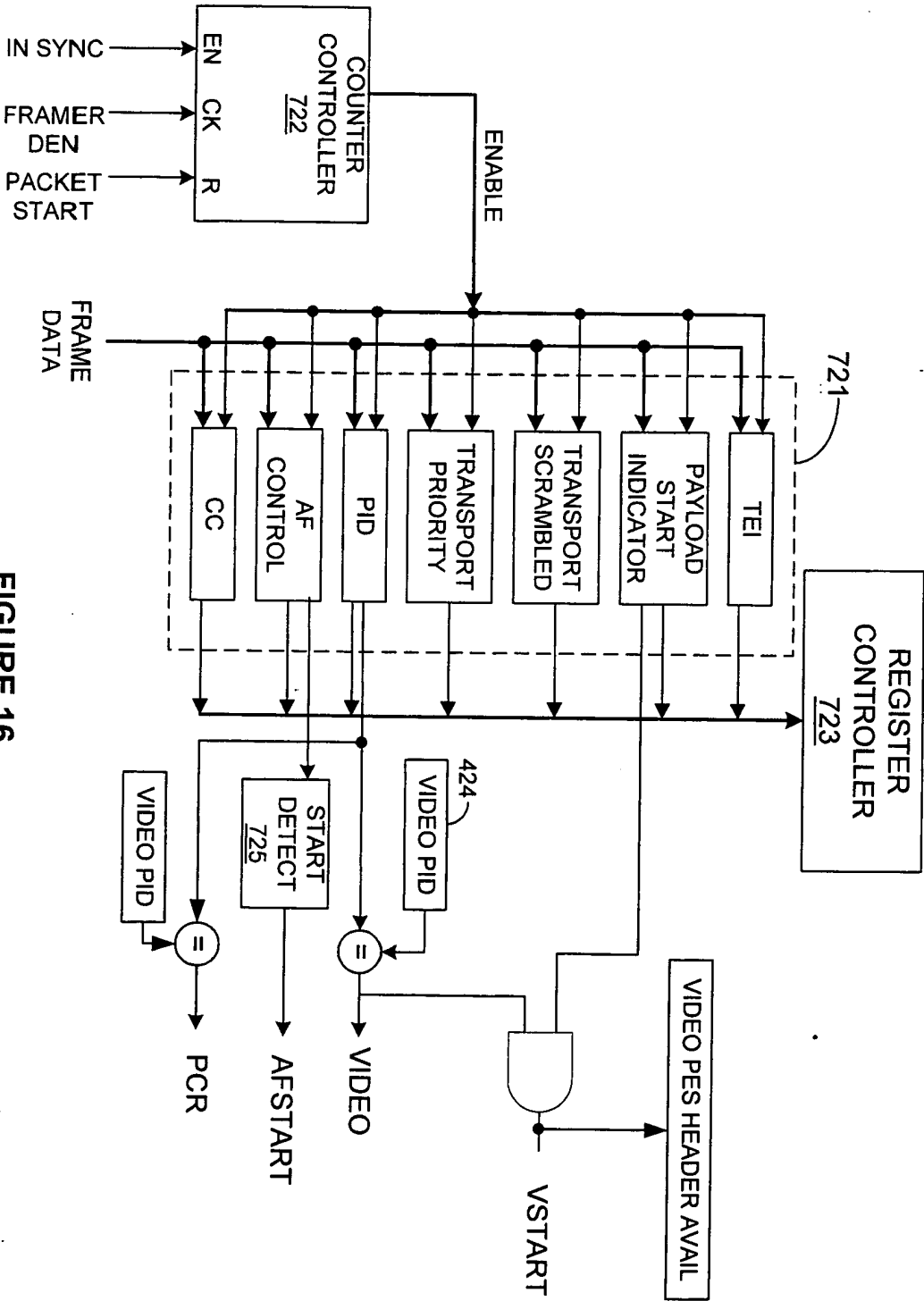


FIGURE 16

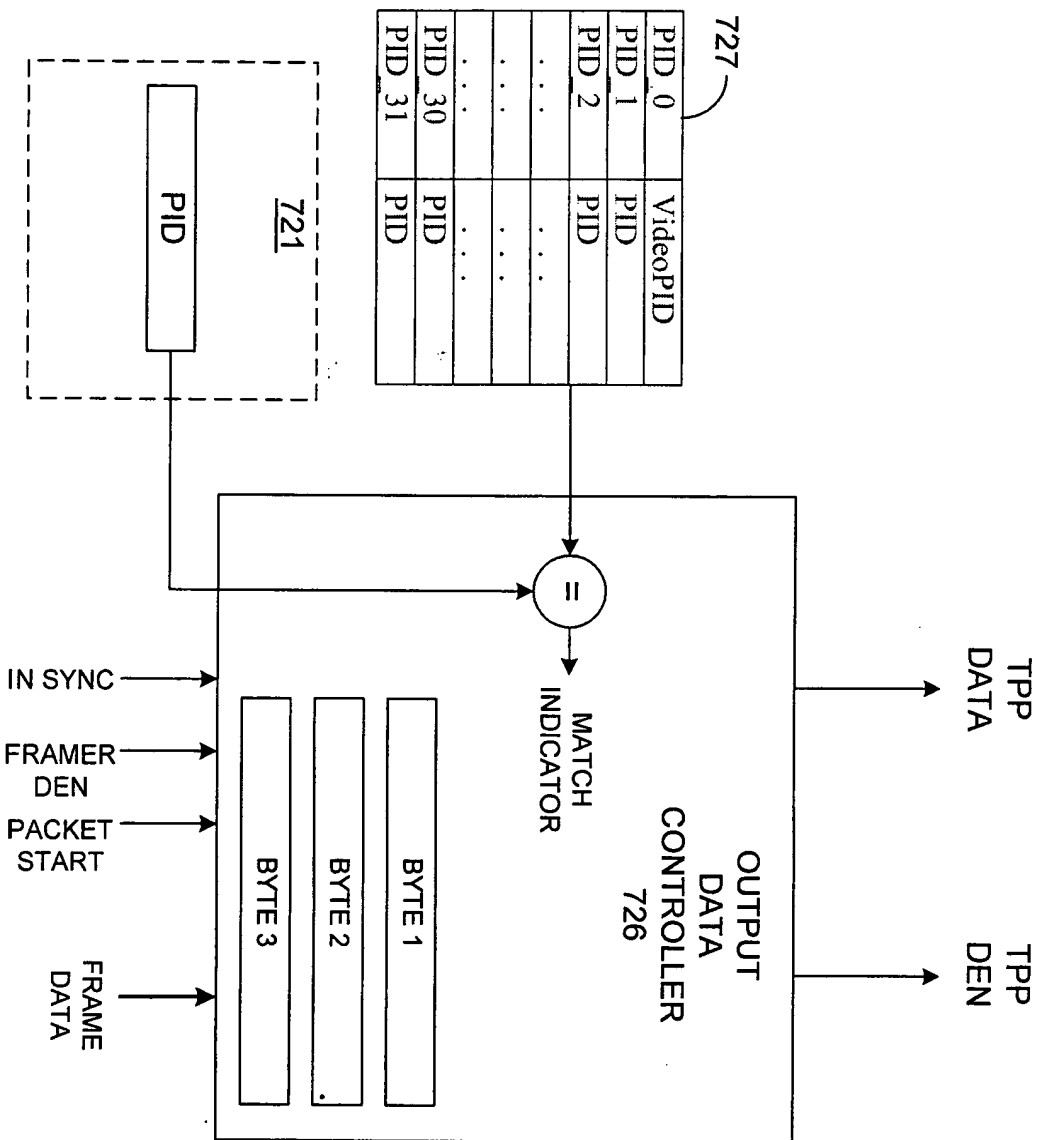


FIGURE 17

Video Control Registers					
Field Name	Bits	Len	Default	Type	Description
VideoPid	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the video component stream to filter on. Value of 4095 is reserved one (it means a NULL transport packets).
EnableParsing	13	[1]	0	R/W	If '1' enables parsing from the next transport packet.
StartFromPUSICommand	14	[1]	0	R/W	'0' enables PES parsing immediately. '1' enables PES parsing a transport packet from new PES packet. After that, this bit auto-returns to 0.
ProcessStreamID	15	[1]	0	R/W	If '1' enables parsing on specific stream_id field.
StreamID	16-23	[8]	0xE0	R/W	stream_id of the ES stream to filter on in the PESP.

FIGURE 18

Transport Demultiplexer Registers					
Field Name	Bits	Len	Default	Type	Description
PID_yz, 0 ≤ yz ≤ 30	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the component stream to filter on. Value of 0x1FFF is reserved (it means a NULL transport packets).
EnableParsing	13	[1]	0	R/W	If set to '1' extraction of defined PID_yz is enabled.
BufferIndex	14-17	[4]	0	R/W	Specifies 1 of 16 destination buffers in the sys. mem.

FIGURE 19

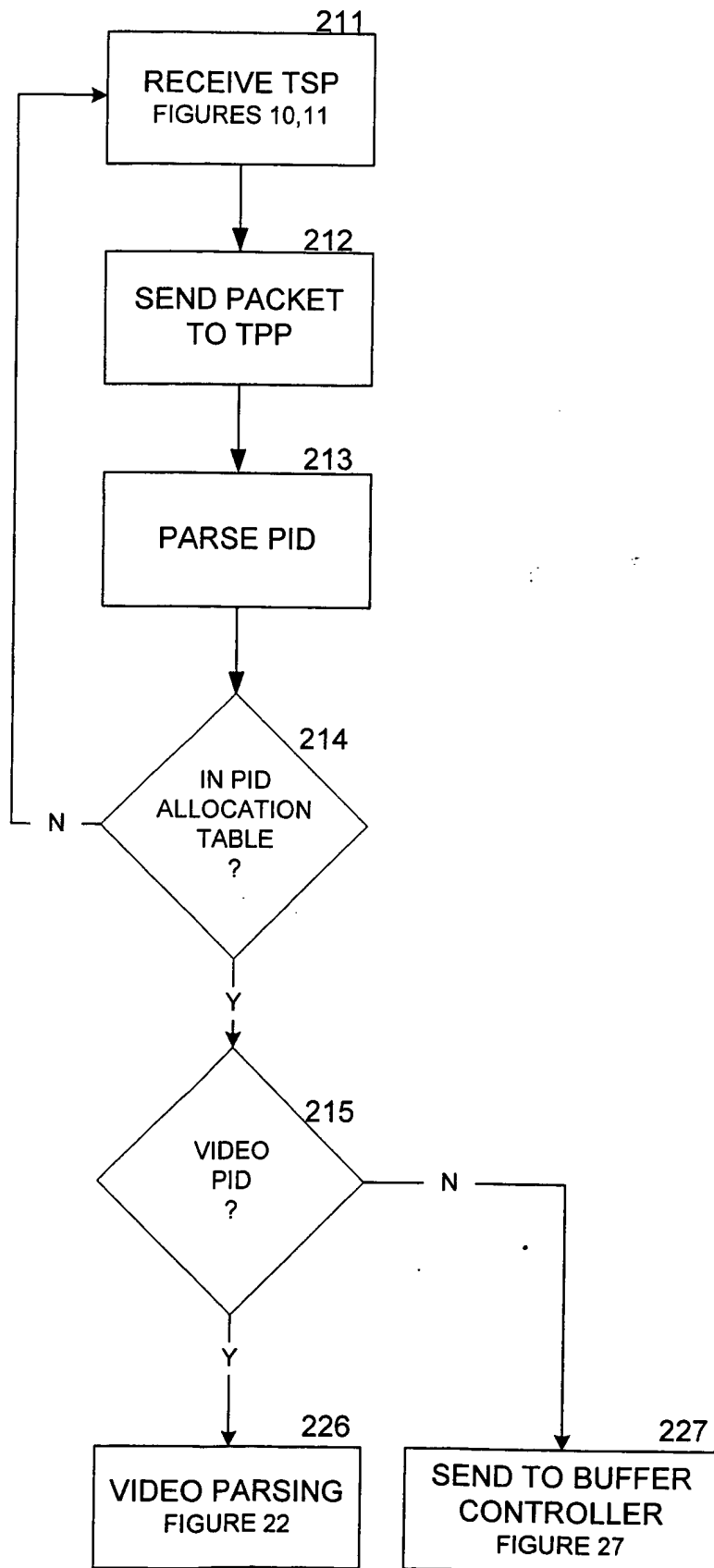


FIGURE 20

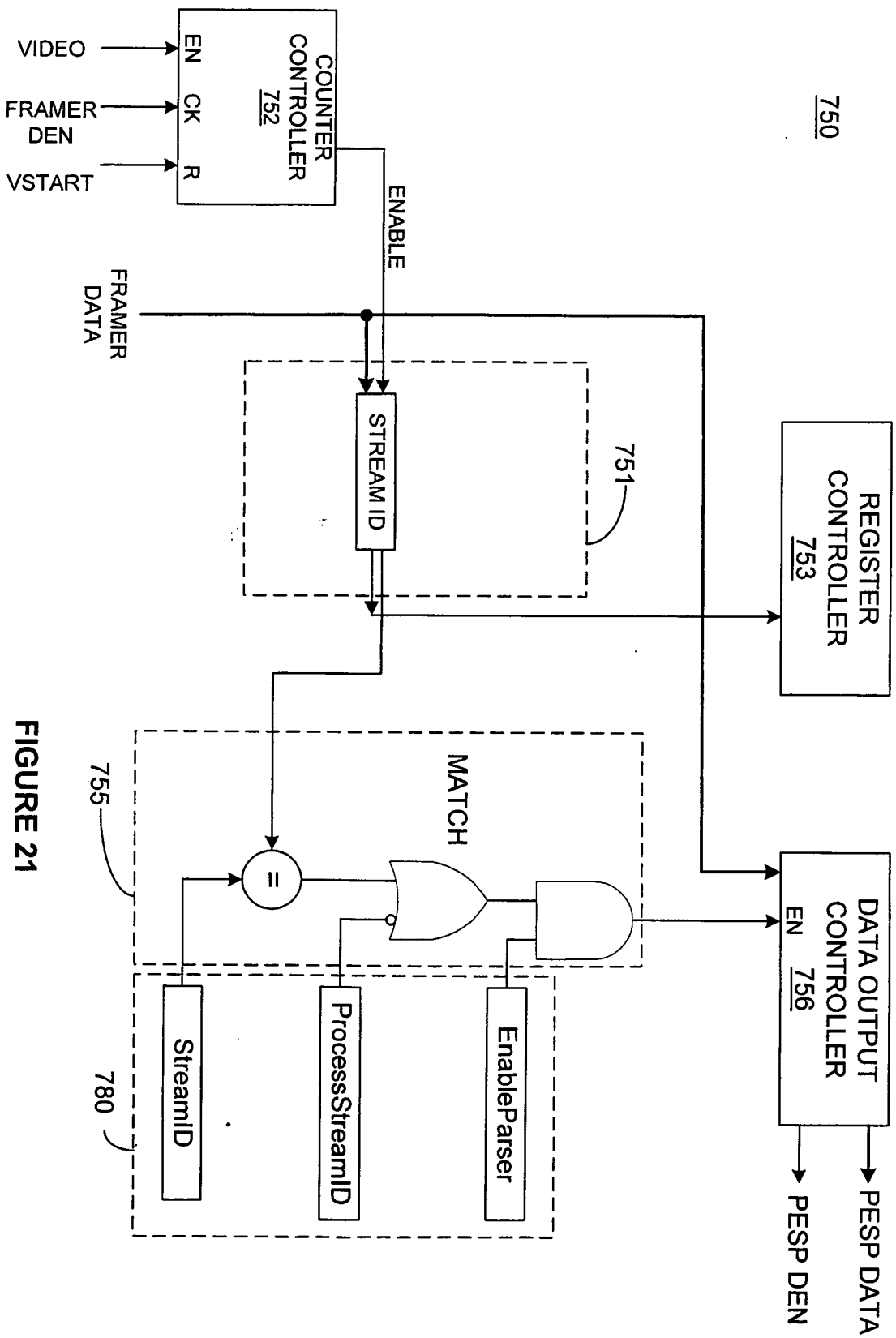


FIGURE 21

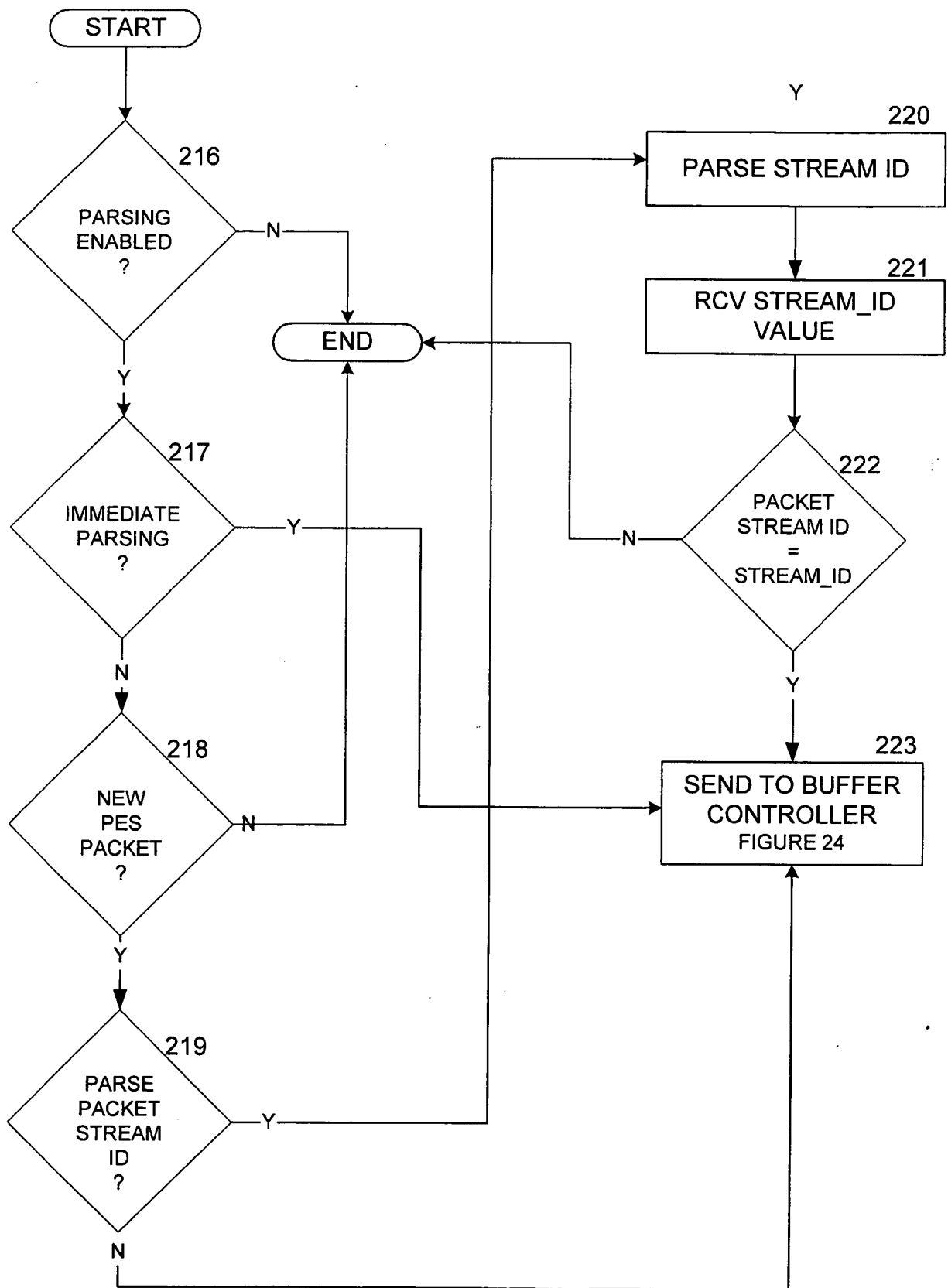


FIGURE 22

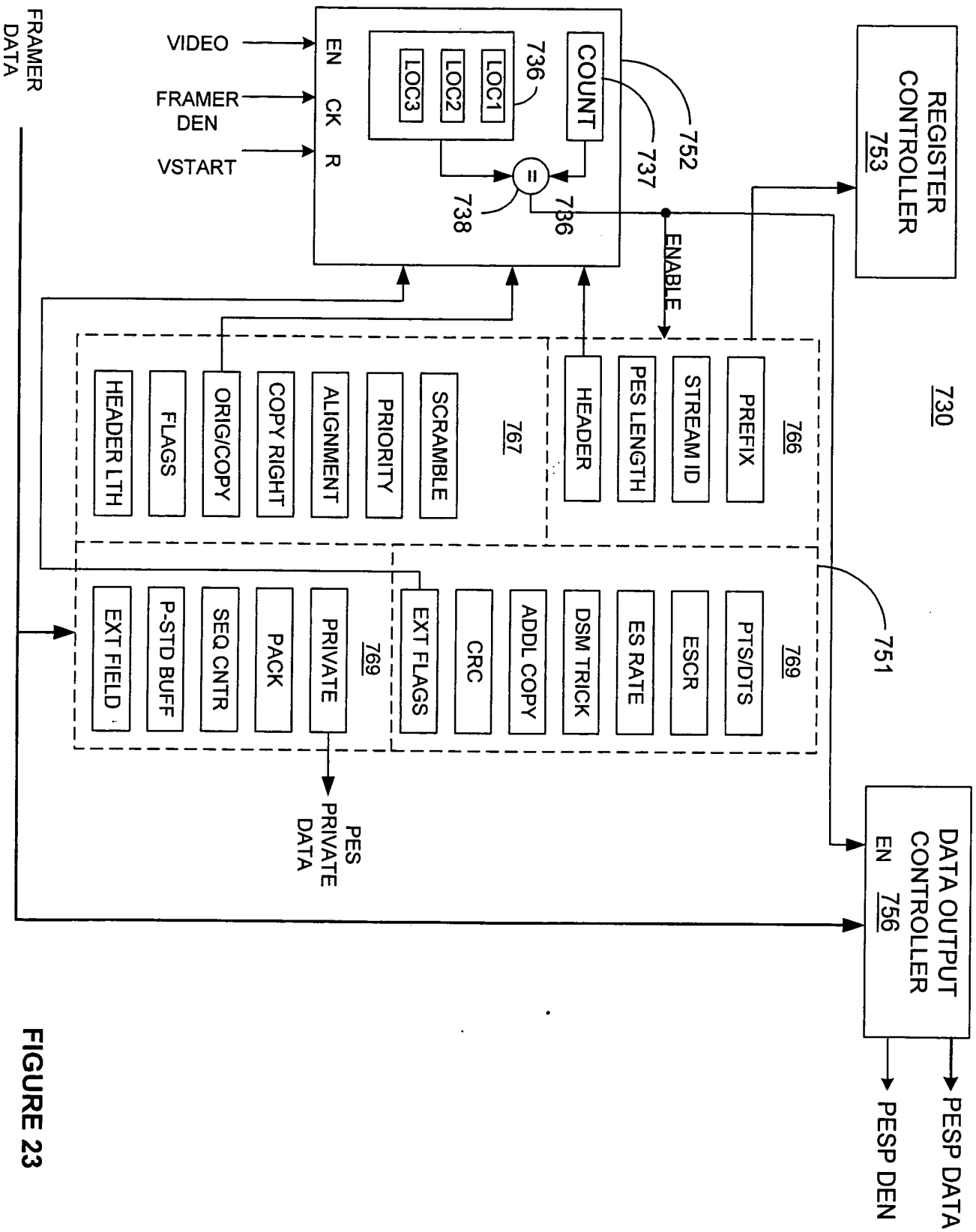


FIGURE 23

Transport Demultiplexer Global Status Register				
Field Name	Bits	Len	Default	Type
VideoPESHeaderAvailable	12	[1]	0	R/W
VideoPESHeaderError	13	[1]	0	R/W
VideoPESDataAlignment	14	[1]	0	R/W
VideoPESDSMTrickMode	15	[1]	0	R/W
VideoPESPrivateData	16	[1]	0	R/W
VideoPESCRCErr	17	[1]	0	R/W

Figure 24

Transport Demultiplexer Interrupt Mask Register				
Field Name	Bits	Len	Default	Type
EventInterruptMask	0-18	[19]	0	R/W

Figure 25

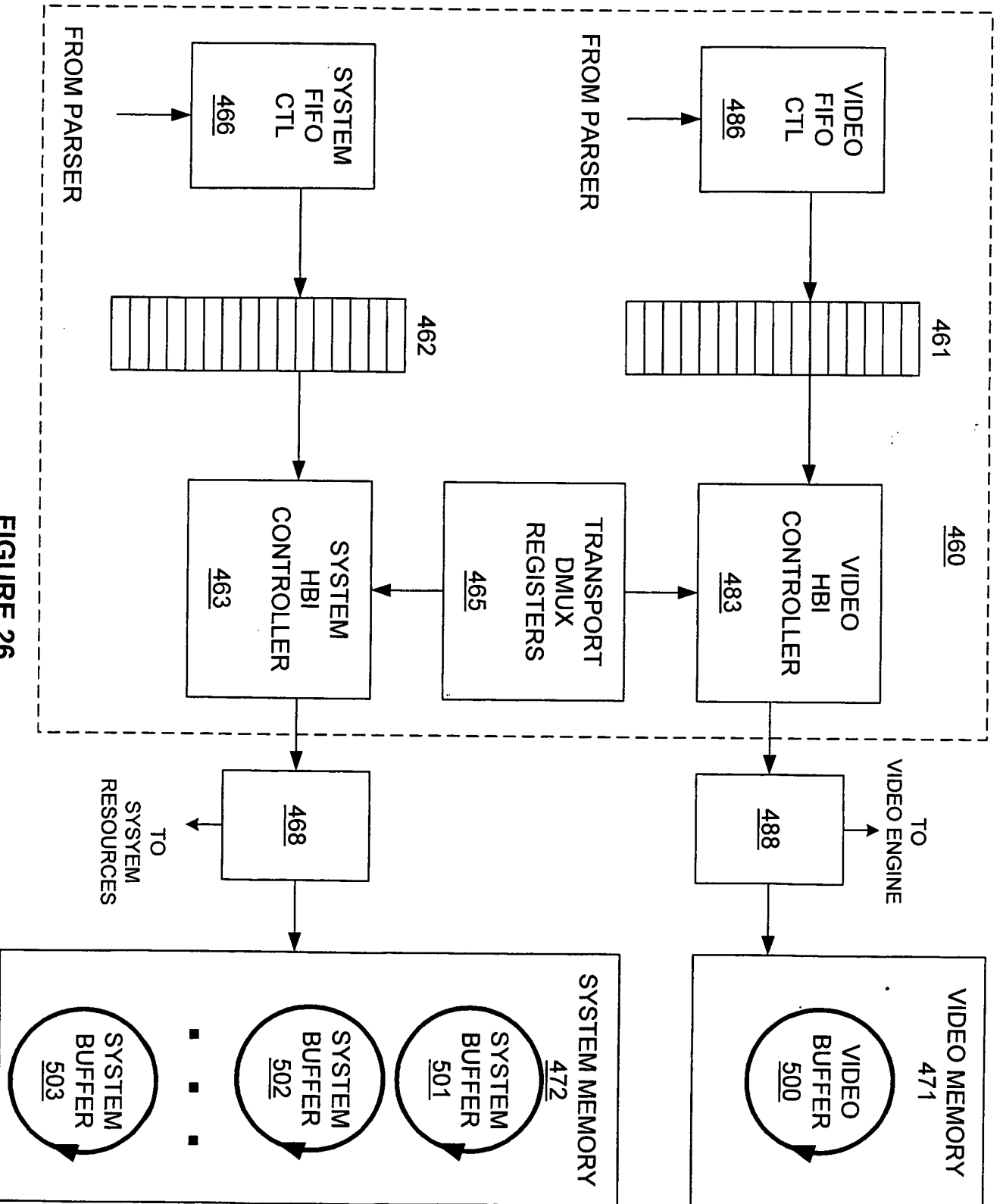


FIGURE 26

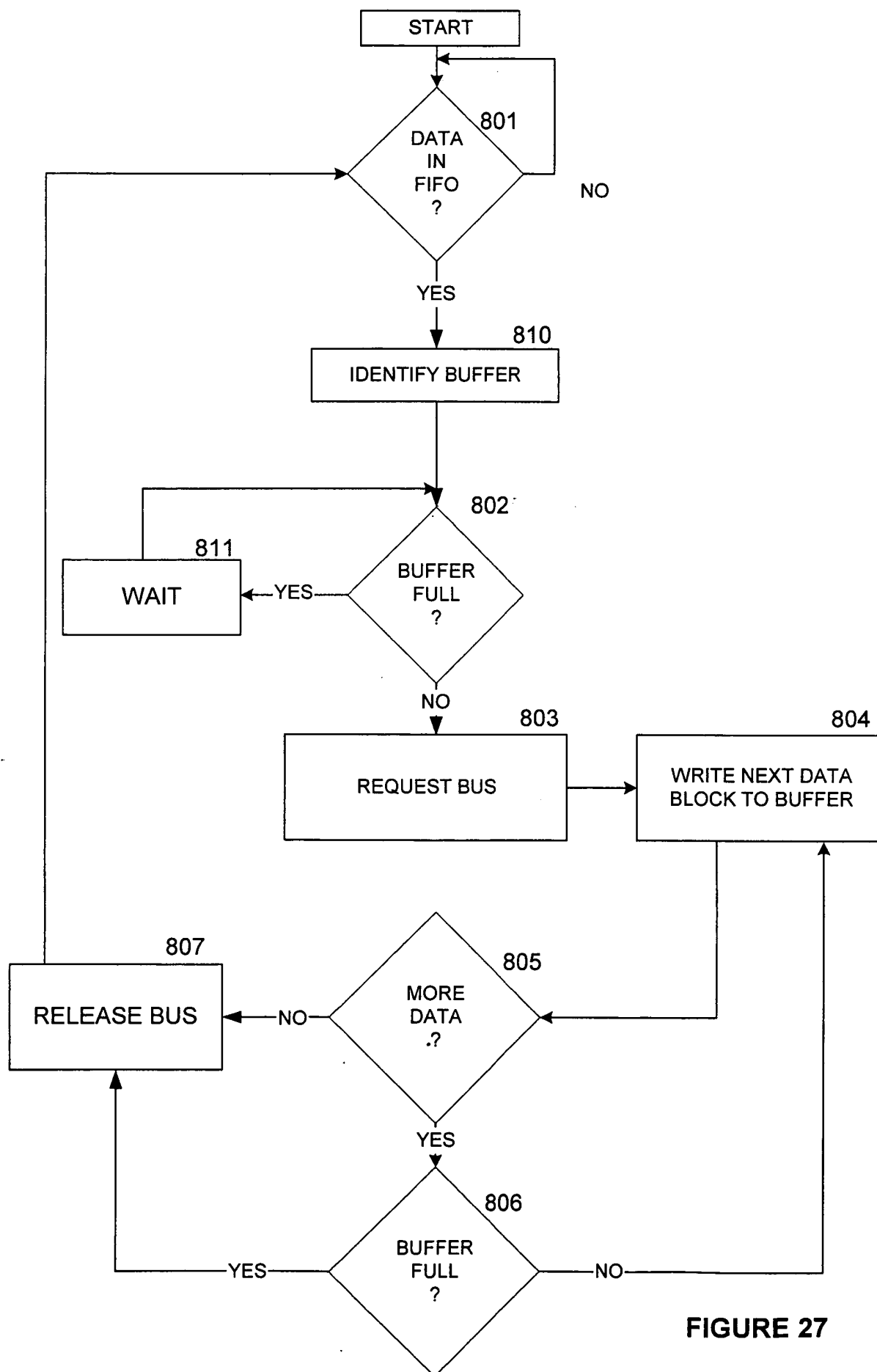


FIGURE 27

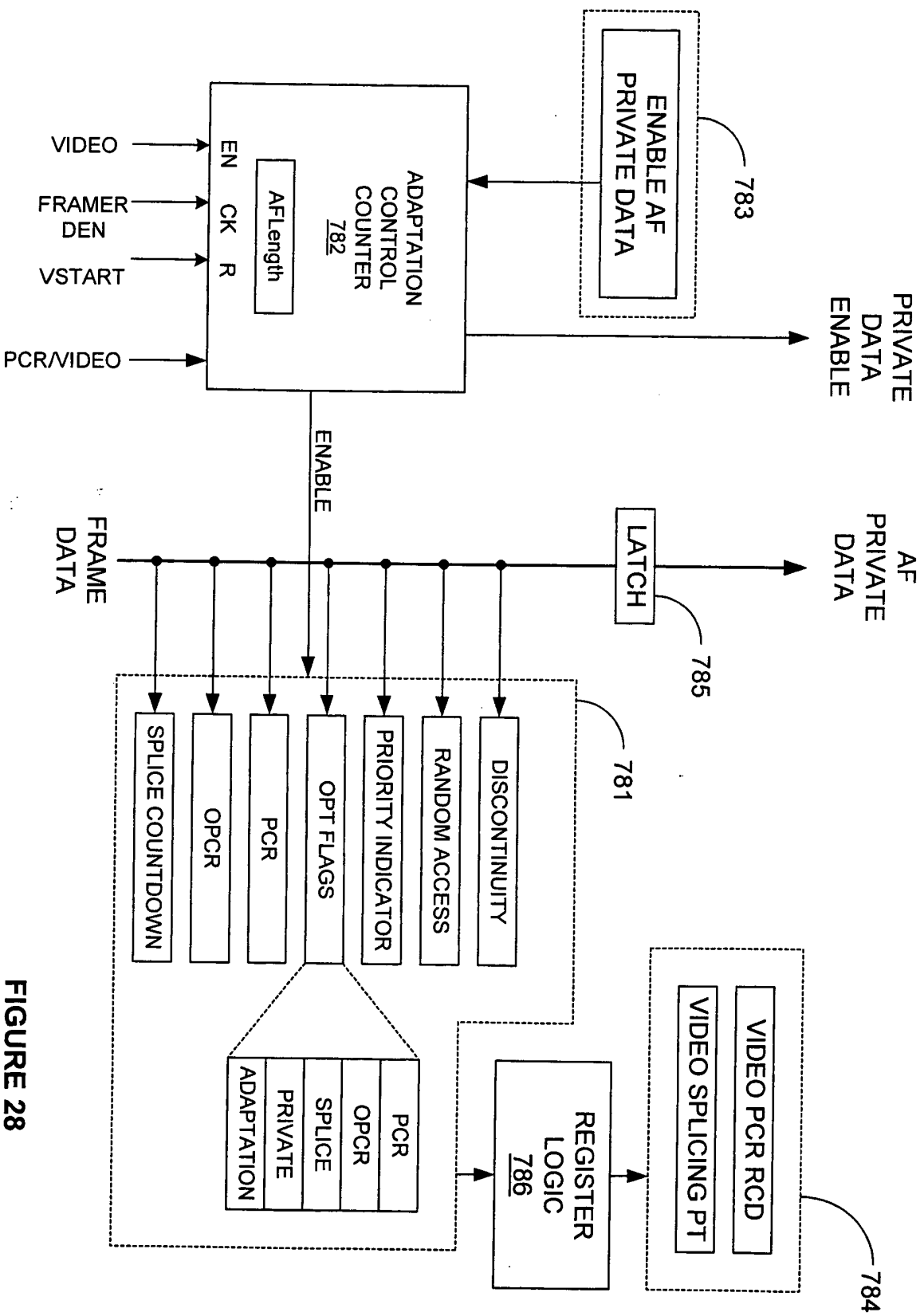


FIGURE 28

Transport Demultiplexer Global Status Register					
Field Name	Bits	Len	Default	Type	Description
VideoAFPcrReceived	[1]		0	R/W	This bit is set to '1' after arrival and extraction of PCR sample in the adaptation field. WR_ACC_CLEAR.
VideoAFPcrDiscontinuity	[1]		0	R/W	This bit is set to '1' when a <i>discontinuity_indicator</i> in the adaptation field of the PCR PID is asserted. WR_ACC_CLEAR.
VideoAFDiscontinuityFlag	[1]		0	R/W	This bit is set to '1' after a <i>discontinuity_indicator_flag</i> has been asserted in the AF of video TP, indicating a discontinuity on continuity_counter. WR_ACC_CLEAR.
VideoAFRandomAccess	[1]		0	R/W	This bit is set to '1' when video PID <i>has random_access_flag</i> asserted in the AF, indicating a start of the elementary stream. WR_ACC_CLEAR.
VideoAFSplicingFlag	[1]		0	R/W	This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, indicating approaching of the splicing point. WR_ACC_CLEAR.
VideoAFSplicingPoint	[1]		0	R/W	This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, after splicing point occurred (splice_countdown =0). WR_ACC_CLEAR.
VideoAFPrivateData	[1]		0	R/W	This bit is set to '1' when video has AF private data. WR_ACC_CLEAR.
AFSpliceCountdown	[8]		0x00	R/W	Current splice countdown value from adaptation field of A/V packets. Modified on the fly by AF content

Figure 29

Transport Demultiplexer Interrupt Mask Register					
Field Name	Bits	Len	Default	Type	Description
EventInterruptMask	0-18	[19]	0	R/W	If set to '1' enables local sources Bit 5 – VideoAFPcrReceived Bit 6 – VideoAFPcrDiscontinuity Bit 7 – VideoAFDiscontinuityFlag Bit 8 – VideoAFRandomAccessFlag Bit 9 – VideoAFSplicingFlag Bit 10 – VideoAFSplicingPoint Bit 11 – VideoAFPrivateData

Figure 30

Transport Demultiplexer Global Control Register				
Field Name	Bits	Len	Default	Type
EnableAFPrivateData	[1]	0		R/W
AFPrivateDataBufferIndex	[4]	0		R/W
PCRIndex	[1]	0		R/W
EnableAutoSplicing	[1]	0		R/W
Description				
If '1' enables parsing and routing of AF private data				
Specifies 1 of 15 destination buffers in the system memory				

Figure 31

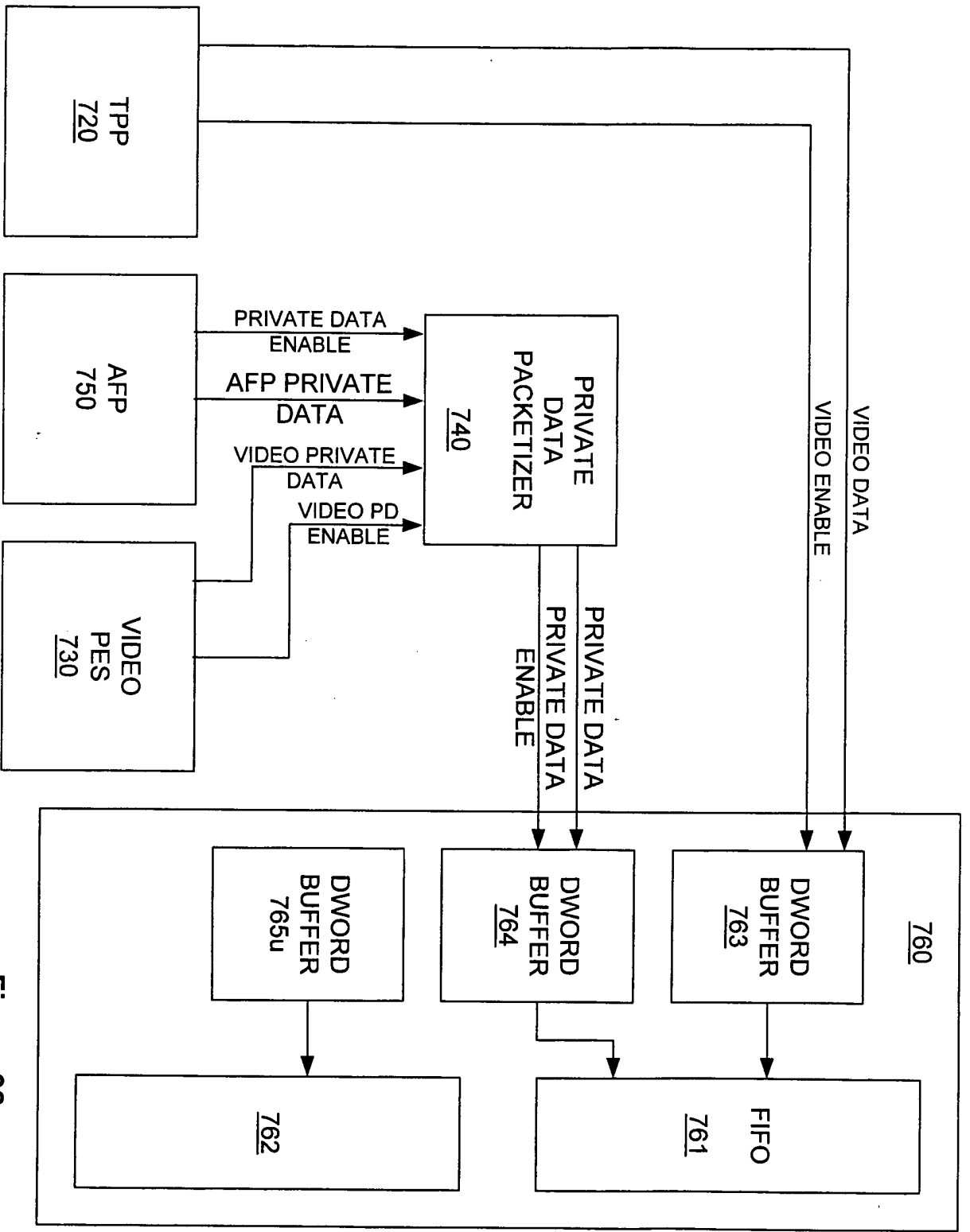


Figure 32

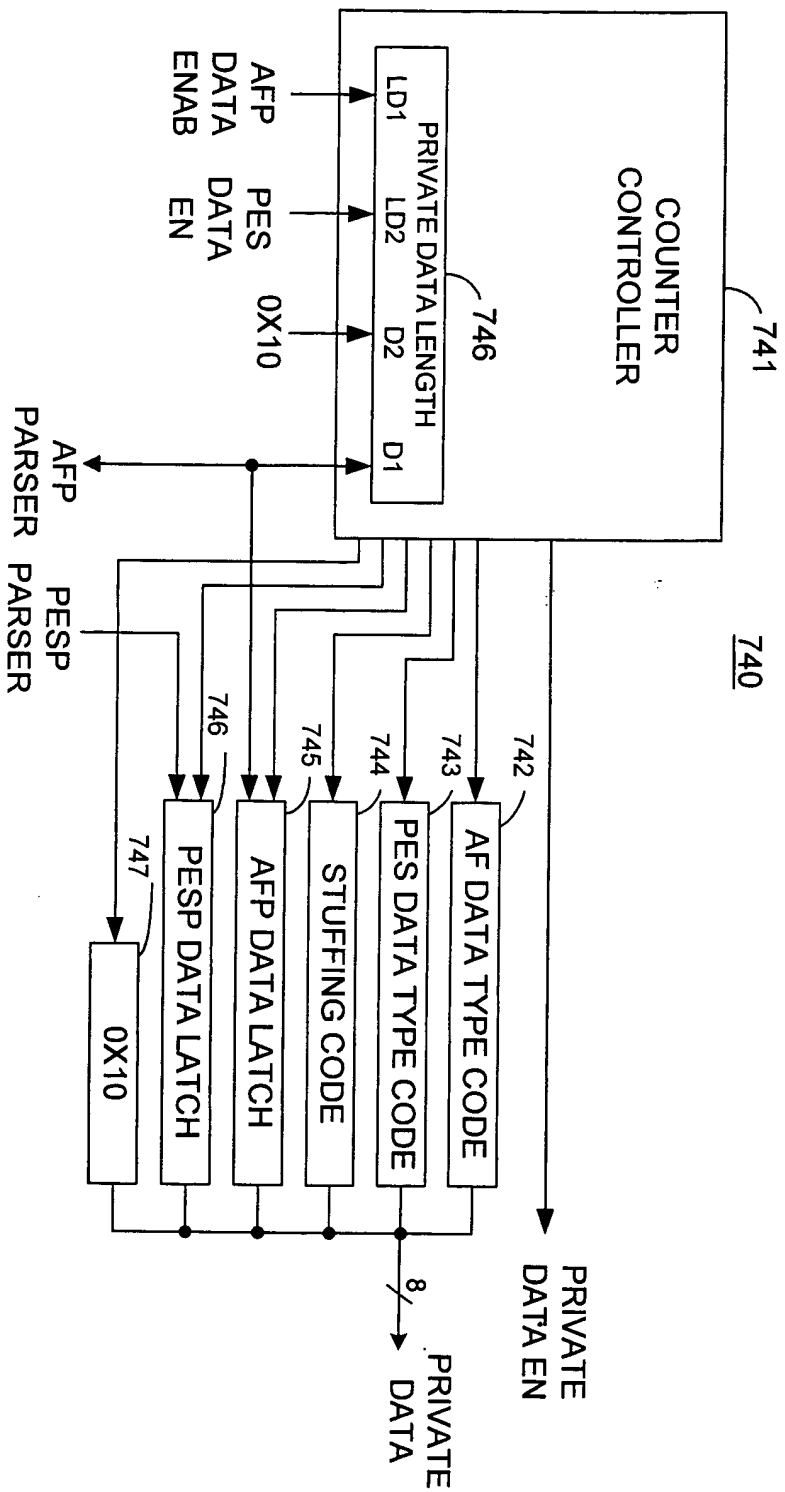


Figure 33

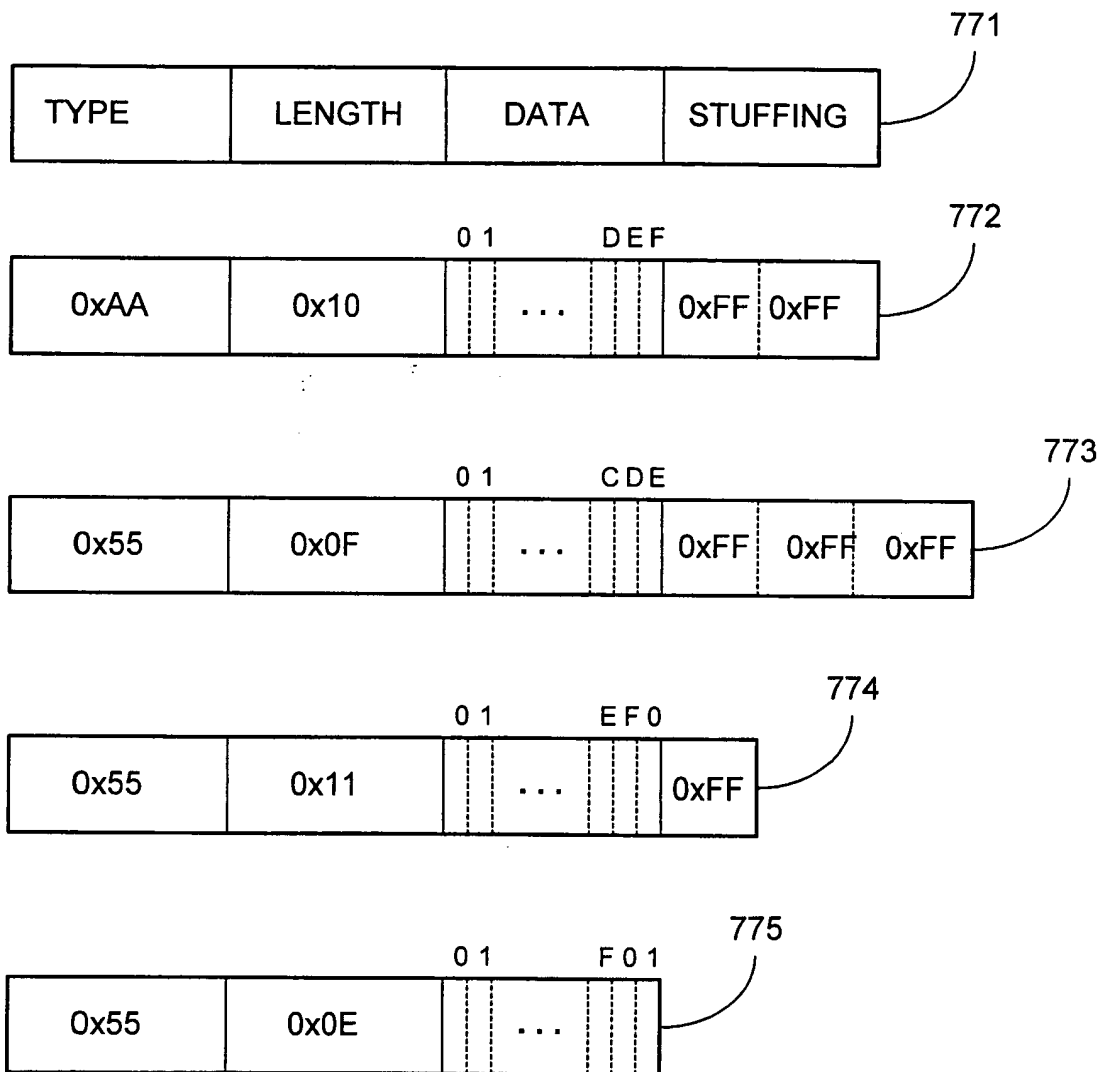


Figure 34

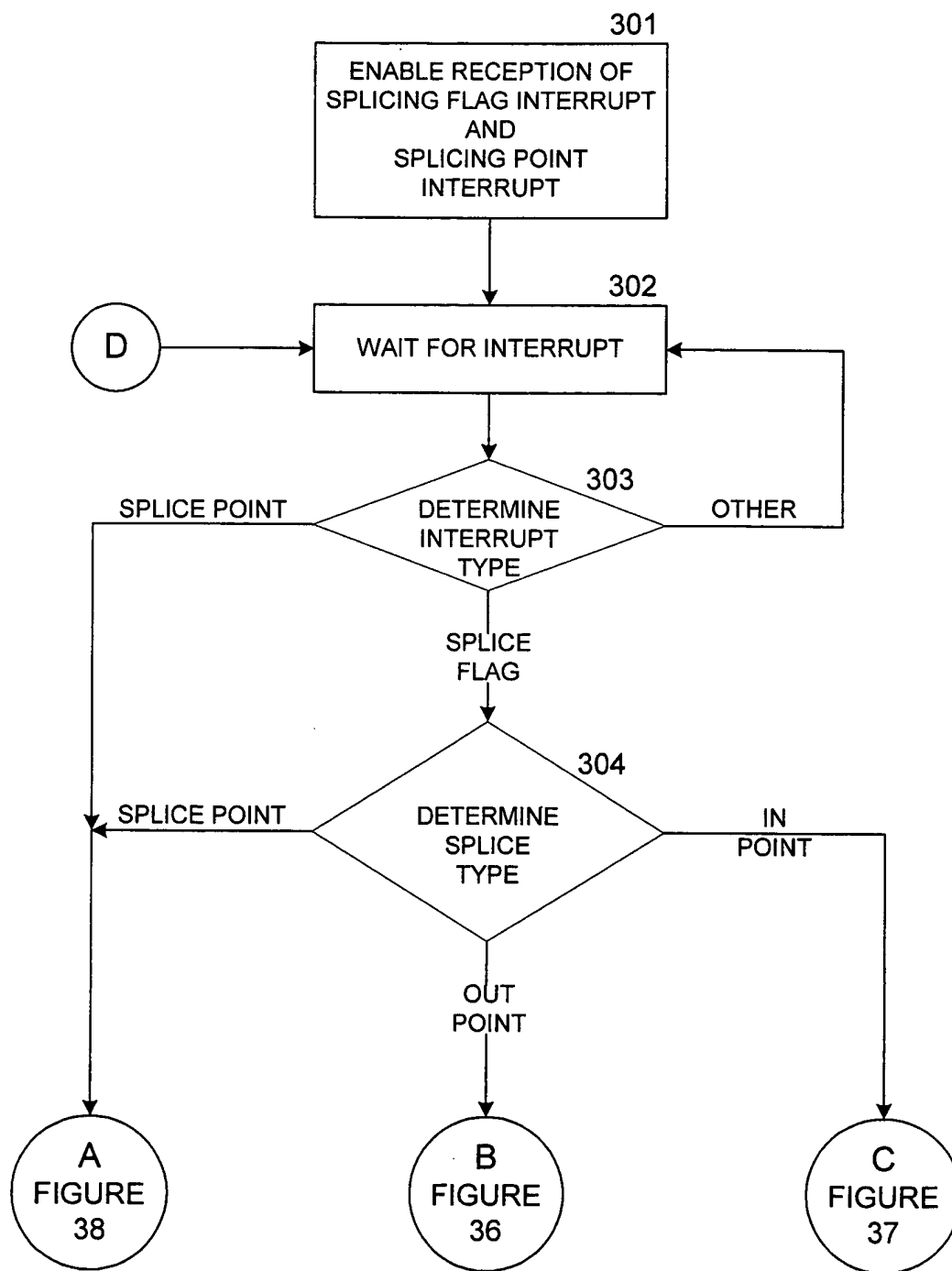


FIGURE 35

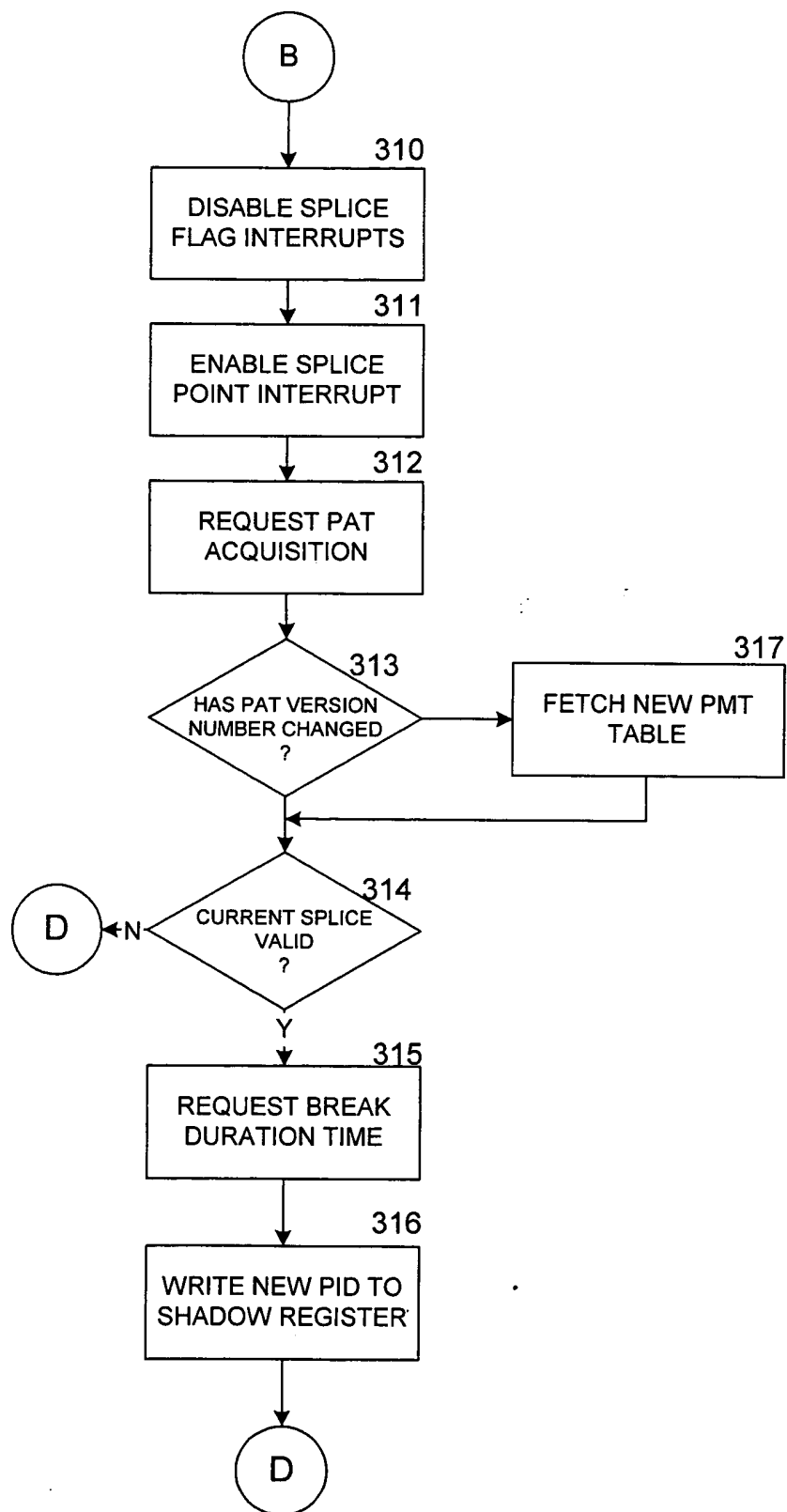


FIGURE 36

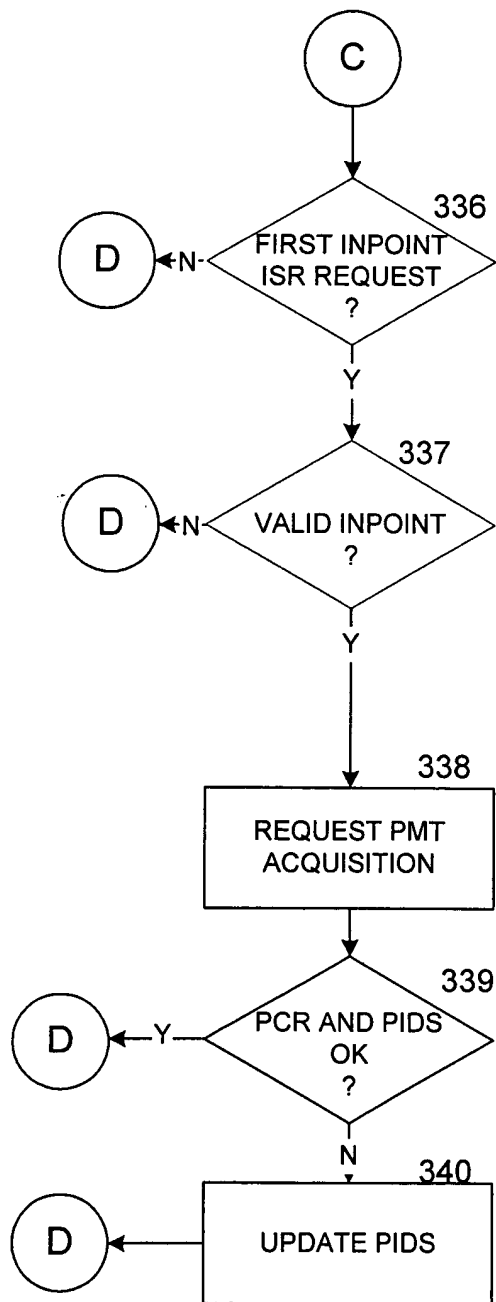


FIGURE 37

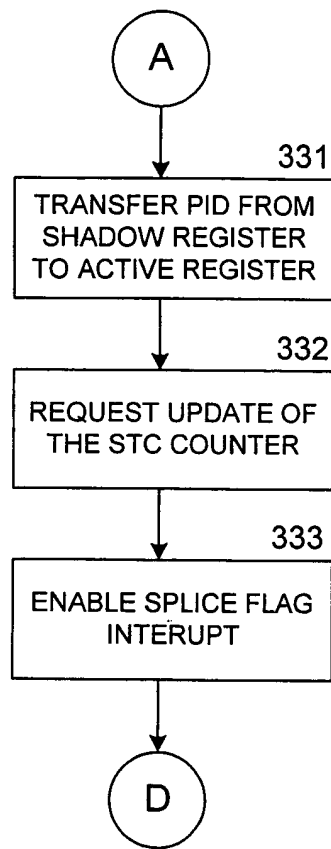


FIGURE 38

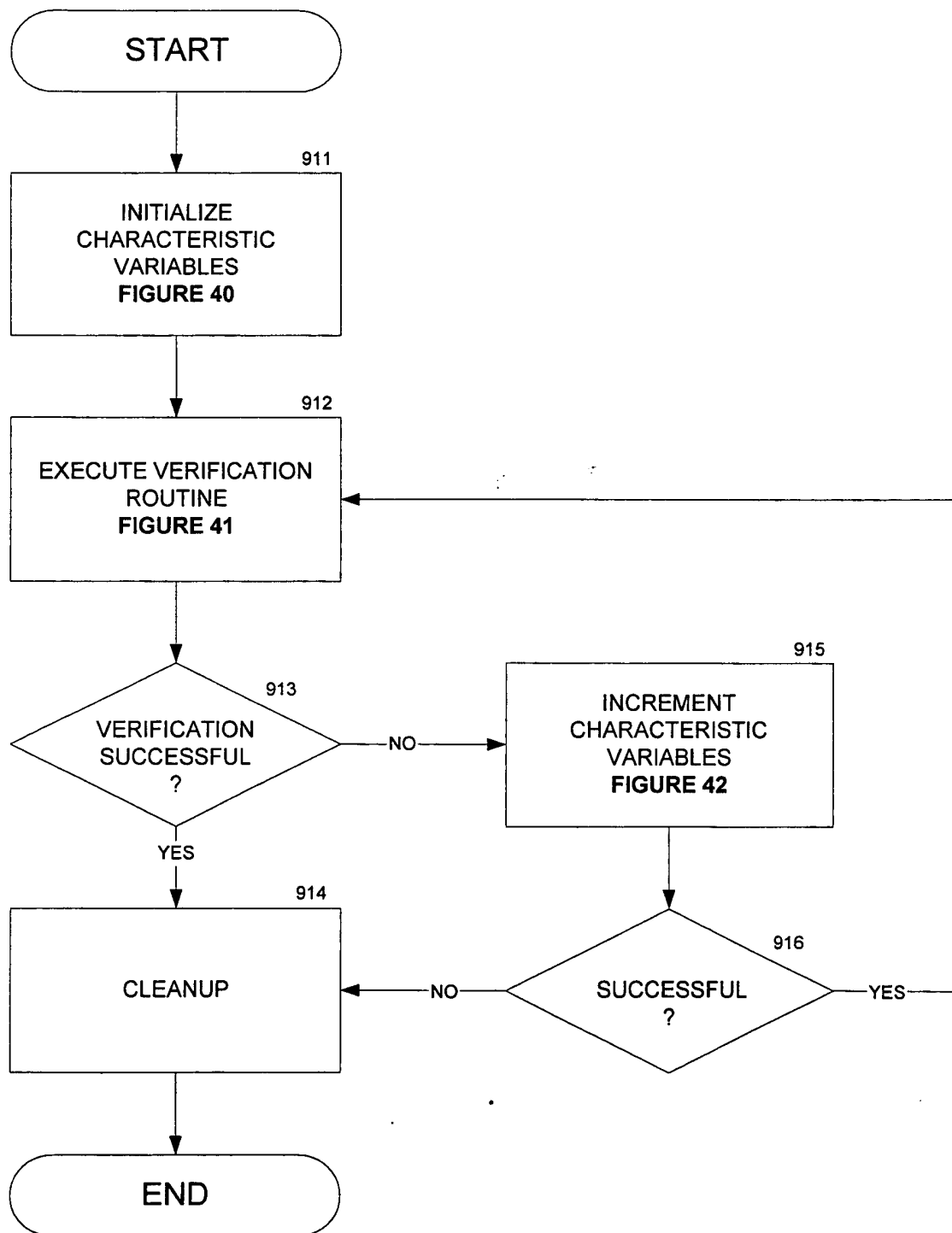


FIGURE 39

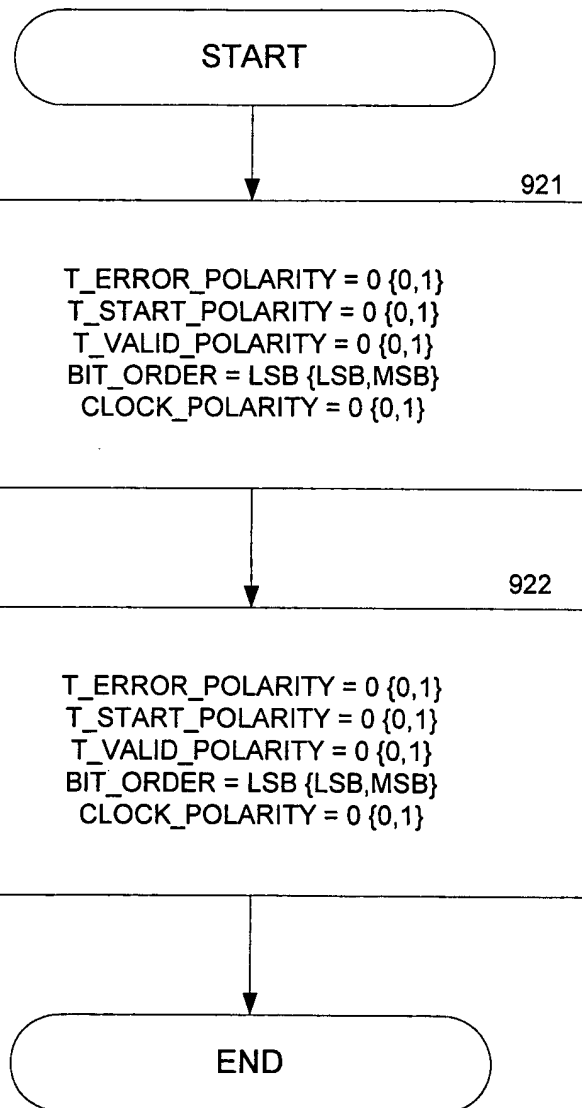


FIGURE 40

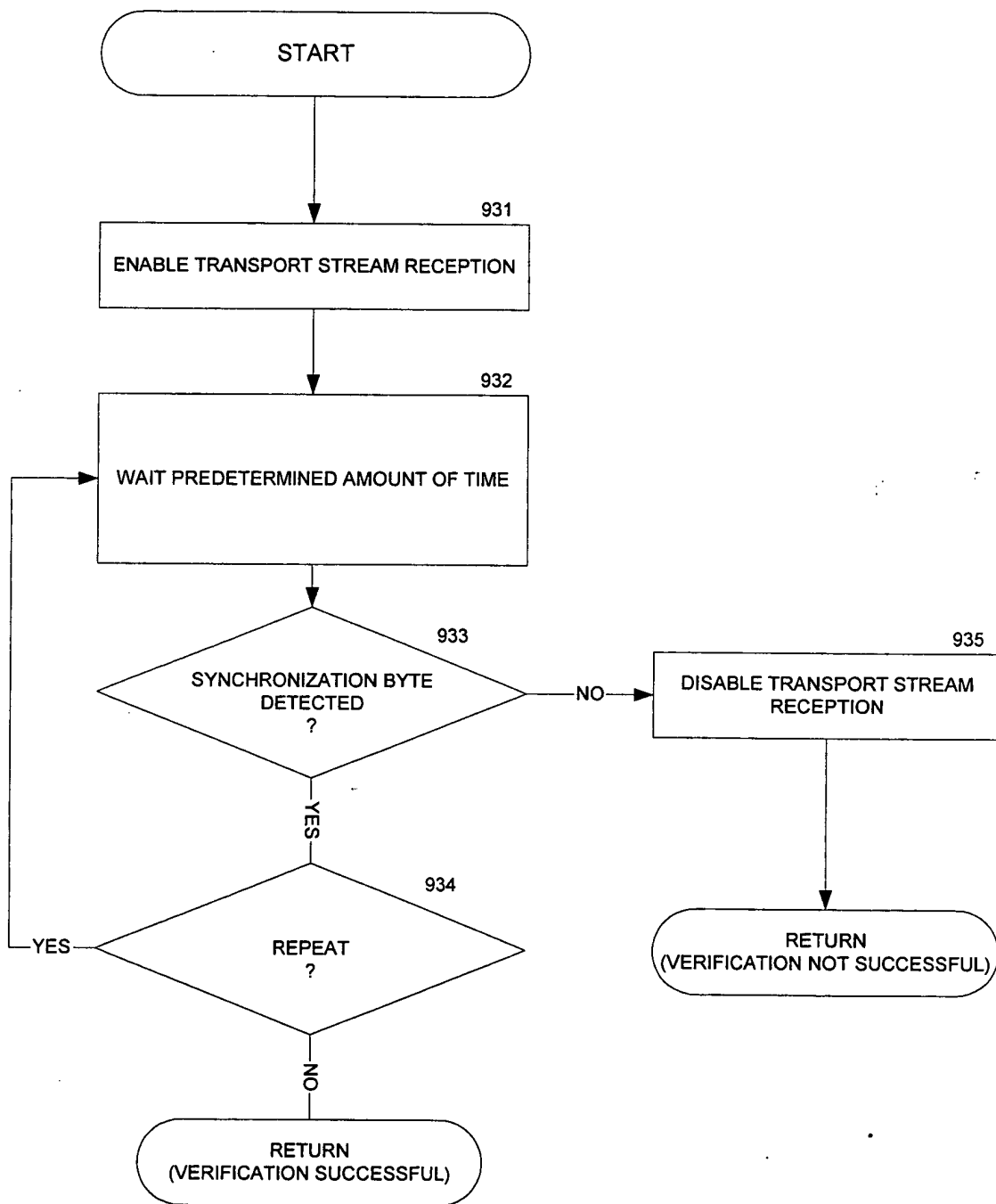


FIGURE 41

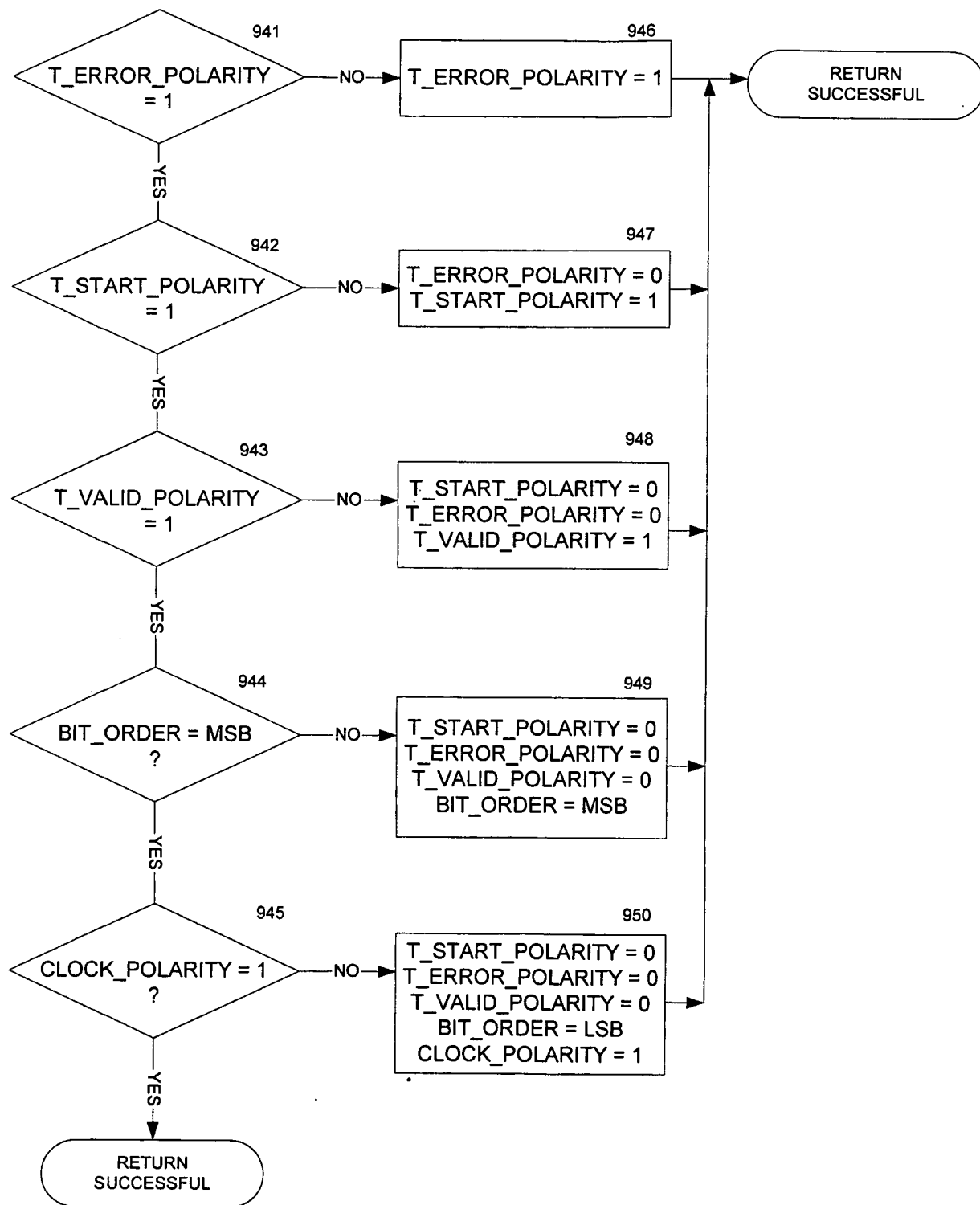


FIGURE 42

1000

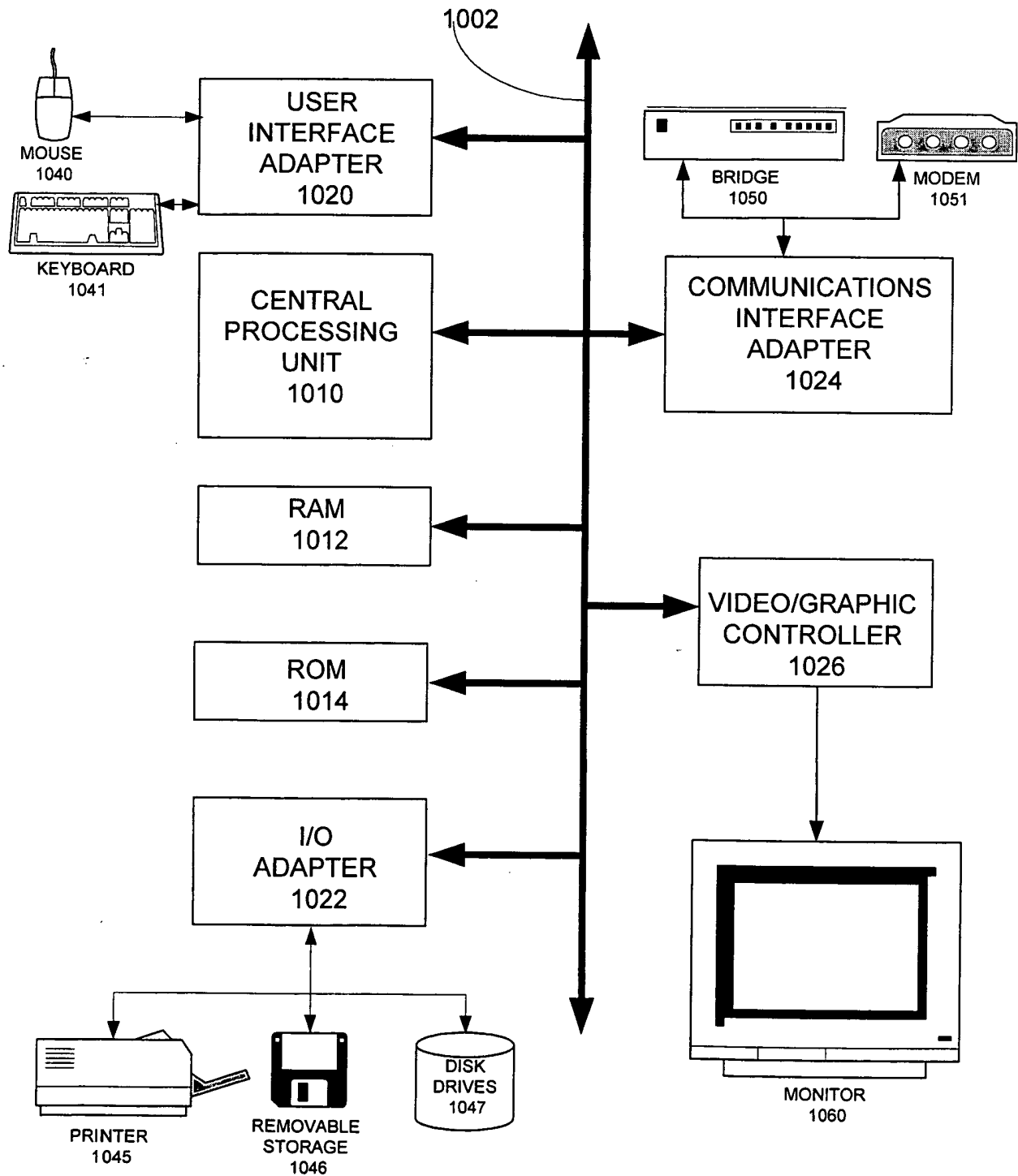


FIGURE 43